

# TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371

Filed: February 8, 1999

U.S. APPLICATION NO. (If known, see 37 CFR 1.5)

09/242046

INTERNATIONAL APPLICATION NO.

INTERNATIONAL FILING DATE

PRIORITY DATE CLAIMED

INT/JP96/02226

August 7, 1996

TITLE OF INVENTION

SEMICONDUCTOR DEVICE AND ITS MANUFACTURING METHOD

414,500,000 00 FEB 1999

APPLICANT(S) FOR DO/EO/US Masahiko HIRATANI, Keiko ABDELGHAFAR, Kazuyoshi TORII, Hiroshi MIKI,  
Yuuichi MATSUI, Yoshihisa FUJISAKI, Kazushige IMAGAWA, Kazumasa TAKAGI

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. ☒ This is a **FIRST** submission of items concerning a filing under 35 U.S.C. 371.
2. ☐ This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. 371.
3. ☐ This express request to begin national examination procedures (35 U.S.C. 371(f)) at any time rather than delay examination until the expiration of the applicable time limit set in 35 U.S.C. 371(b) and PCT Articles 22 and 39(1).
4. ☒ A proper Demand for International Preliminary Examination was made by the 19th month from the earliest claimed priority date.
5. ☒ A copy of the International Application as filed (35 U.S.C. 371(c)(2))
  - a. ☐ is transmitted herewith (required only if not transmitted by the International Bureau).
  - b. ☒ has been transmitted by the International Bureau.
  - c. ☐ is not required, as the application was filed in the United States Receiving Office (RO/US).
6. ☒ A translation of the International Application into English (35 U.S.C. 371(c)(2)).
7. ☒ Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371(c)(3))
  - a. ☐ are transmitted herewith (required only if not transmitted by the International Bureau).
  - b. ☐ have been transmitted by the International Bureau.
  - c. ☐ have not been made; however, the time limit for making such amendments has NOT expired.
  - d. ☐ have not been made and will not be made.
8. ☐ A translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3)).
9. ☒ An oath or declaration of the inventor(s) (35 U.S.C. 371(c)(4)).
10. ☒ A translation of the annexes to the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371(c)(5)).

Items 11. to 16. below concern document(s) or information included:

11. ☒ An Information Disclosure Statement under 37 CFR 1.97 and 1.98.
12. ☒ An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.
13. ☐ A **FIRST** preliminary amendment.  
☐ A **SECOND** or **SUBSEQUENT** preliminary amendment.
14. ☐ A substitute specification.
15. ☐ A change of power of attorney and/or address letter.
16. ☒ Other items or information:  
International Publication No. W098/06131 - Coversheet  
International Search Report  
Change of Correspondence Address  
Figures: 1-6, 7a-7b, 8a-8c, 9, 10a-10b, 11-20  
Information Disclosure Statement Under 37 CFR 1.97 & 1.98

PCT/JP96/02226

501.36894X00

17. ☒ The following fees are submitted:

## BASIC NATIONAL FEE (37 CFR 1.492(a)(1)-(5)):

Search Report has been prepared by the EPO or JPO ..... \$ 840.00

International preliminary examination fee paid to USPTO (37 CFR 1.482) ..... \$ 670.00

No international preliminary examination fee paid to USPTO (37 CFR 1.482) but international search fee paid to USPTO (37 CFR 1.445(a)(2)) ..... \$ 490.00

Neither international preliminary examination fee (37 CFR 1.482) nor international search fee (37 CFR 1.445(a)(2)) paid to USPTO ..... \$ 700.00

International preliminary examination fee paid to USPTO (37 CFR 1.482) and all claims satisfied provisions of PCT Article 33(2)-(4) ..... \$ 96.00

## CALCULATIONS PTO USE ONLY

840.00

## ENTER APPROPRIATE BASIC FEE AMOUNT =

\$ 840.00

Surcharge of \$130.00 for furnishing the oath or declaration later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492(e)).

\$

CLAIMS	NUMBER FILED	NUMBER EXTRA	RATE
Total claims	36 - 20 =	16	X 18.00
Independent claims	6 - 3 =	3	X 78.00

\$ 288.00

\$ 234.00

MULTIPLE DEPENDENT CLAIM(S) (if applicable)

+ 260.00

\$

## TOTAL OF ABOVE CALCULATIONS =

\$ 1,362.00

Reduction of 1/2 for filing by small entity, if applicable. Verified Small Entity Statement must also be filed (Note 37 CFR 1.9, 1.27, 1.28).

\$

## SUBTOTAL =

\$ 1,362.00

Processing fee of \$130.00 for furnishing the English translation later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492(f)).

\$

## TOTAL NATIONAL FEE =

\$ 1,362.00

Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31). \$40.00 per property

\$

40.00

## TOTAL FEES ENCLOSED =

\$ 1,402.00

Amount to be:

refunded

\$

charged

\$

a. ☒ A check in the amount of \$ 1,402.00 to cover the above fees is enclosed.b. ☐ Please charge my Deposit Account No. \_\_\_\_\_ in the amount of \$ \_\_\_\_\_ to cover the above fees. A duplicate copy of this sheet is enclosed.c. ☒ The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. 01-2135. A duplicate copy of this sheet is enclosed.

NOTE: Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137(a) or (b)) must be filed and granted to restore the application to pending status.

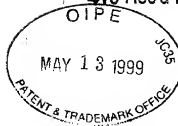
SEND ALL CORRESPONDENCE TO:

ANTONELLI, TERRY, STOUT & KRAUS, LLP  
 1300 NORTH SEVENTEENTH STREET  
 SUITE 1800  
 ARLINGTON, VA 22209

SIGNATURE:

Gregory E. Montone  
 NAME

28,141  
 REGISTRATION NUMBER



501.36894X00

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

Applicant(s): M. HIRATANI, et al

Serial No.: 09/242,046

Filed: February 8, 1999

For: SEMICONDUCTOR DEVICE AND ITS MANUFACTURING METHOD

Group:

Examiner:

**PRELIMINARY AMENDMENT**Assistant Commissioner for Patents  
Washington, D.C. 20231

May 13, 1999

Sir:

The following preliminary amendments and remarks are respectfully submitted in connection with the above-identified application.

**IN THE SPECIFICATION:**

Please replace the original specification with the attached Substitute Specification.

**IN THE CLAIMS:**

Please amend the claims as follows:

Claim 1, line 6, delete "form ed" insert --formed--;  
line 9, after "layer" insert --,--;

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line 13, delete "differently" insert --are  
different--;

line 16, delete "includes" insert --has an--.

Claim 3, line 1, delete "semiconductor" insert  
--semiconductor--;

line 4, delete "with" insert --having an--;

line 5, delete "that are".

Claim 4, line 5, delete "with" insert --having an--;

line 6, delete "that are".

Claim 5, line 5, delete "with" insert --which has an--;

line 6, after "type" insert --of--;

line 7, after "group" insert --consisting--.

Claim 6, line 4, after "type" insert --of--.

Claim 7, line 4, after "type" insert --of--.

Claim 8, line 3, delete "with" insert --having--;

line 5, delete "by" insert --in--.

9. (amended) A semiconductor device in accordance with  
claim 1, wherein

an oxide composing said [double] double-layered  
conductive oxide layer consists of at least one type of  
compound selected from a group consisting of  $\text{CaRuO}_3$ ,  $\text{SrRuO}_3$ ,  
and  $\text{SrTiO}_3$  to which La is added by over 0.5 weight % to 4.0  
weight% (included), and all of [them having the] which have a  
perovskite structure.

10. (amended) A [semicond uctor] semiconductor device in accordance with claim 1, wherein

an oxide composing said double-layered conductive oxide layer has a mixed phase of at least one type of compound selected from a group consisting of  $\text{CaRuO}_3$ ,  $\text{SrRuO}_3$ , and  $\text{SrTiO}_3$  which La is added by over 0.5 weight% to 4.0 weight% (included), and all of [them having the] which have a perovskite structure, with an [alkalline] alkaline-earth metal oxide composing said compound, that is, CaO or SrO.

Claim 11, line 3, delete "with sai d" insert --having said--;

line 5, delete "by" insert --in--.

Claim 13, line 3, delete "conduct I've" insert --conductive--; same line 3, delete "with" insert --having--;

line 4, delete "said"; same line 4, delete "by" insert --in--;

line 7, delete " $\text{ReO}_3$ " insert -- $\text{ReO}_3$ --.

Claim 14, line 3, delete "with" insert --having--.

17. (amended) A method for manufacturing a semiconductor device, including a process for forming a conductive oxide layer [with] having an oxygen deficiency, [by] comprising the steps of sputtering or evaporating elements composing said conductive oxide in a non-oxidizing atmosphere, and then forming a conductive oxide layer on said conductive oxide

layer [with] having said oxygen deficiency, thereby forming a lower electrode layer on a substrate; a process for forming an oxide dielectric layer on said lower electrode layer; and a process for forming an upper electrode layer on said oxide dielectric layer, wherein

said lower electrode layer consists mainly of two conductive oxide layers formed in the same crystal structure and consisting of the same element, but different from each other in oxygen composition ratio, and

said lower and upper electrode layers, as well as said oxide dielectric layer, are combined thereby composing an oxide dielectric capacitor.

Claim 18, line 1, delete "for" insert --of--.

Claim 19, line 1, delete "for" insert --of--.

Claim 20, line 1, delete "for" insert --of--;

line 3, delete "with" insert --having--;

line 5, delete "the" insert --a--;

line 6, delete "the" insert --a--;

line 7, after "is" insert --in--.

21. (amended) A method [for] of manufacturing a semiconductor device in accordance with claim 17, wherein

said conductive oxide layer [with] having said oxygen deficiency, which is formed in said double-layered conductive oxide layer, is then formed with [the] a sputtering method or

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[the] a vacuum deposition method, and said non-oxidizing atmospheric gas consists of at least one type of gas selected from oxygen [(O<sub>2</sub>)] (O<sub>2</sub>), nitric monoxide [(N<sub>2</sub>O)] (N<sub>2</sub>O), nitric dioxide (NO<sub>2</sub>), and ozone (O<sub>3</sub>), and the pressure or partial pressure of said gas is 10 μTorr or below.

Claim 22, line 9, after "layer" insert --,--.

Claim 23, line 1, delete "devic e" insert --device--.

Claim 26, line 3, after "type" insert --of--;

line 4, after "group" insert --consisting--.

Claim 27, line 3, after "type" insert --of--;

line 4, delete "of IrO<sub>2</sub>" and insert --consisting of IrO<sub>3</sub>--.

Claim 28, line 1, delete "accor dance" and insert --accordance--;

line 4, delete "Ti<sub>1-x</sub>Al<sub>x</sub>)<sub>1</sub>." insert

--(Ti<sub>1-x</sub>Al<sub>x</sub>)<sub>1-y</sub>N<sub>y</sub>--;

line 5, delete "N<sub>y</sub>".

Claim 29, line 1, delete "accordanc e" insert --accordance--.

31. (amended) A method [for] of manufacturing a semiconductor device, [including;] comprising:

a step [for] of forming a lower electrode layer including an aluminum titanium nitride layer on a substrate by sputtering in a nitridizing atmosphere;

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a step [for] of forming an oxide dielectric layer on said lower electrode layer; and

a step [for] of forming an upper electrode layer on said oxide dielectric layer, wherein

both lower and upper electrode layers, as well as said oxide dielectric layer, are combined thereby composing an oxide dielectric capacitor.

Claim 32, line 1, delete "for" insert --of--.

Claim 33, line 1, delete "for" insert --of--;

line 4, delete "preventing" insert --prevents--;

line 5, after "oxidation" insert --and--.

Claim 34, line 1, delete "for" insert --of--;

line 4, delete "preventing" insert --to prevent--.

35. (amended) A semiconductor device, including[;]:

a first area consisting of a semiconductor material; a second area connected to said first area and consisting of [said] a first conductive material; a third area connected to said second area and consisting of [said] a second conductive material; a fourth area connected to said third area and consisting of an oxide dielectric material; and a fifth area connected to said fourth area and consisting of a conductive material, wherein



the material composition at the interface of said first area adjacent to said second area is approximately equal to the average material composition of said first area, and the material compositions at the interface of said second area adjacent to said first area, as well as to said third area, is approximately equal to the average material composition of said second area.

36. (amended) A semiconductor device, including[;]:

a first area [consi sting] consisting of a conductive semiconductor material; a second area connected to said first area and consisting of [said] a first conductive material; a third area connected to [said] a second area and consisting of said second conductive material; a fourth area connected to said third area and consisting of an oxide dielectric material; and a fifth area connected to said fourth area and consisting of a conductive material, wherein

the average resistivity of said first area is approximately equal to the resistivity of said semiconductor material and the average resistivity of said second area is approximately equal to the resistivity of said first conductive material.

**IN THE ABSTRACT OF THE DISCLOSURE:**

Delete line 2, and insert --A--;

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668120 44024200

line 3, delete "for" insert --of--; same line 3,  
delete "that";

line 4, after "and" insert --is able--;

line 5, after "of" (first occurrence) insert --a--;

line 7, after "11," insert --an--; same line 7,  
delete "dielectrics" insert --dielectric layer--;

line 11, delete "These" insert --The--;

line 12, delete "in" insert --to have--; same line  
12, delete "with" insert --are of--;

line 14, delete "includes" insert --has an--;

line 15, delete "including" insert --which has an--;

line 17, after "interface" insert --,--;

line 18, delete "oxidation" insert --oxidizing--.

#### REMARKS

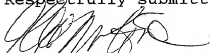
The specification has been amended to correct errors of a typographical and grammatical nature. Due to the excessive corrections thereto, applicants submit herewith a Substitute Specification, along with a marked-up copy of the original specification for the Examiner's convenience. Applicants submit that the substitute specification includes the changes as shown in the marked-up copy and includes no new matter. Therefore, entry of the Substitute Specification is respectfully requested.

The claims and abstract have also been amended to more clearly describe the features of the present invention and to correct the grammatical nature therein.

Entry of the preliminary amendments and examination of the application is respectfully requested.

To the extent necessary, applicant's petition for an extension of time under 37 CFR 1.136. Please charge any shortage in the fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account No. 01-2135 (501.36894X00) and please credit any excess fees to such deposit account.

Respectfully submitted,



Gregory E. Montone  
Registration No. 28,141  
ANTONELLI, TERRY, STOUT & KRAUS, LLP

GEM/DRA/cee  
Attachments  
(703) 312-6600

0042015.021899

SUBSTITUTE SPECIFICATION

Title of the Invention

SEMICONDUCTOR DEVICE AND ITS MANUFACTURING METHOD

Technical Field

5 The present invention relates to a semiconductor device which is suitable for LSIs, as well as a method of manufacturing such a semiconductor device. The semiconductor device uses oxide dielectrics, especially oxide ferroelectrics in the formation of a capacitor.

Background of the Invention

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Semiconductor devices consisting of LSIs such as dynamic random access memories (DRAMs), etc. have been confronted with problems that the capacitor area must be reduced to cope with high integration of the LSI. In addition, such a semiconductor device must be prevented from having a complicated structure caused by the reduction of such the capacitor area. In order to solve these problems, therefore, consideration has been given to the use of oxide dielectrics and oxide ferroelectrics as the insulator of the capacitor, instead of silicon oxide and silicon nitride, which have been used so far. The relative dielectric constants of both oxide dielectrics and oxide ferroelectrics are as large as several hundreds to several thousands. (The oxide dielectrics mentioned here do not include silicon oxides, but concern so-called dielectrics whose relative dielectric constants are several hundreds.) The ferroelectrics have spontaneous polarization and a polarity

that can be reversed using an external electric field. The reversed polarity can also be held. It has thus been proposed to use such ferroelectrics for non-volatile memories. A conventional memory composed of such ferroelectrics is disclosed in the official gazette of Unexamined Published Japanese Patent Application No-Sho-63-201998 (since oxide ferroelectrics can be regarded as dielectrics at temperatures above the Curie temperature, hereunder, the term dielectrics will be used to describe the ferroelectrics representatively).

Generally, lead zirconate titanate, strontium barium titanate, and the like are used as oxide dielectrics for memories. However, it has been difficult to use oxide dielectric capacitors for semiconductor devices used as conventional memories, etc., since high temperatures above 500°C are needed to crystallize the oxide dielectrics in an oxidizing atmosphere.

For example, it might be considered to adopt a structure (conventional structure 1; oxide dielectrics/platinum/silicon) such that platinum can be used for a lower electrode which is resistant against both oxidation and thermal budget, provided under an oxide dielectric capacitor. However, platinum and silicon react with each other to form platinum silicide at their interface. Consequently, the electrical resistance of each electrode increases. Thus, the (conventional structure 1) allowing such a platinum electrode to come directly in contact with both the silicon substrate and polycrystalline silicon will not be suitable. Instead of conventional structure 1,

therefore, another structure was proposed in 1989 IEEE Int. Solid-State Circuits Conf. Digest pp-242-243. In this structure, oxide dielectric capacitors are formed on a passivation layer. On the other hand, a MOS transistor is formed outside the capacitor area. And, a conductive wiring layer using aluminum, and the like is applied to connect the source or drain of the MOS transistor to the capacitor. In the case of this method that uses such a conductive wiring layer, it is difficult to reduce the area of each memory cell, so that the method is not suitable for a memory which is highly integrated.

The official gazette of Unexamined Published Japanese Patent Application No. Hei-3-256358 disclosed a method for highly integrating a memory formed as follows; a semiconductor substrate provided with a MOS transistor formed thereon is coated with an insulating material; and on the substrate an oxide dielectric capacitor is formed. In this method, contact holes are formed in the insulator and a conductive material is filled in the contact holes thereby to connect either the source or the drain of the MOS transistor electrically to one of the two electrodes of the capacitor. Generally, polycrystalline silicon is used as the conductive material to be filled in the contact holes. This structure, however, could not avoid the occurrence of the above problems. In other words, a structure that crystallizes oxide dielectrics directly on polycrystal line silicon (conventional structure 2; oxide dielectrics/polycrystalline silicon) oxidizes the

interface between those materials, thereby forming a reaction insulating layer. On the other hand, in order to prevent the formation of such a reaction insulating layer, the (conventional structure 3; oxide dielectrics/platinum/polycrystalline silicon) is required. In this structure, platinum is inserted between polycrystalline silicon and oxide dielectrics to cope with the problem. This structure is substantially the same as the (conventional structure 1) in configuration. Platinum and polycrystalline silicon react with each other, thereby forming silicide. As a result, the electrical resistance of each electrode increases, and silicon diffuses into the platinum as well, causing a silicon oxide film to be formed on the surface of the platinum, so that the characteristics of the dielectric capacitor are deteriorated. Another problem occurs, in that the elements composing the dielectrics diffuse into the silicon substrate.

In order to solve those problems, the official gazettes of Unexamined Published Japanese Patent Application No. Hei-4-14862 and No. Hei-4-181766 disclosed a (fourth structure 4; oxide dielectrics/platinum/(Ti, Ta, TiN, etc.)/polycrystalline silicon) having a non-oxide anti-diffusion conductive layer (formed with Ti, Ta, TiN, etc.) so as to prevent inter diffusion between the platinum electrode and silicon.

In addition to platinum, Ti, Ta, TiN, etc. used for electrode components, conductive oxides are also used as each electrode of an oxide dielectric capacitor. Such an example is reported in (Journal of Material Research, Vol. 8 (1993),

pp.12). This typical example represents a (fifth structure;  
oxide dielectrics/ruthenium oxide/SiO<sub>2</sub>). If oxide dielectrics  
can be put directly in contact with ruthenium oxide, an  
advantage will be obtained in that the mechanical adhesive  
strength at the interface between oxide dielectrics and  
electrode increases more than when oxide dielectrics is put in  
contact with a completely different type metallic electrode.  
Such an increase of the mechanical adhesive strength between  
oxide dielectrics and the electrode can improve the  
characteristics of the oxide dielectric capacitor, such as the  
polarization cycle, etc. In this example, the capacitor is  
formed on SiO<sub>2</sub>. If the capacitor is formed on polycrystalline  
silicon, however, ruthenium oxide, which is an oxide, should  
not be put in contact directly with polycrystalline silicon  
for the same reasons as in the case of the (conventional  
structure 1) and the (conventional structure 3). And. in order  
to prevent such a direct contact, a noble metallic layer made  
of platinum, ruthenium, and the like should be formed between  
them. In this case, the (conventional structure 6; oxide  
dielectrics/ruthenium oxide/(platinum/ruthenium, etc.)/  
polycrystalline silicon) will be used suitably.

#### Summary of the Invention

In the above related art, description was made of  
conventional technology to be applied to memories to be  
integrated more highly by coating a MOS-transistor-formed-  
semiconductor substrate with an insulating material, and then  
forming an oxide dielectric capacitor thereon. As described



above, the source or drain of the MOS transistor is connected electrically to one of the two electrodes of the capacitor through contact holes, which are generally filled with a conductive material consisting of polycrystal line silicon.

And, the following two structures are adopted for the conventional technology described above:

(Conventional Structure 4)

Oxide dielectrics/platinum/(Ti, Ta, TiN, etc.)/  
polycrystalline silicon

(Conventional Structure 6)

Oxide dielectrics/ruthenium oxide/(platinum, ruthenium,  
etc.)/polycrystalline silicon

Each of the above structures includes the following problems.

At first, the (conventional structure 4) will be described. In order to crystallize oxide dielectrics, an oxidizing atmosphere at 500°C or higher is required. Under such a condition, however, oxygen diffuses along grain boundaries, etc. of platinum crystal grains, to cause oxygen to reach the anti-diffusion non-oxide conductive layer (Ti, Ta, TiN, etc.) to oxidize even that layer. Consequently, the electrical resistance of the electrode itself increases. In order to avoid such a problem, the thickness of the platinum layer is increased. This method, however, makes it difficult to process the platinum layer, and results in an increase in leakage current from the side wall of the capacitor. This is because the aspect ratio of the capacitor increases if the

memory is highly integrated and a fine capacitor is formed. And, this is why the (conventional structure 4) cannot solve the conventional technology problems if Ti, Ta, TiN, etc. are used for an anti-interdiffusion layer.

5       Next, the (conventional structure 6) will be described. Also in this case, the ruthenium oxide layer is usually formed in an oxidizing atmosphere. Oxygen diffusion reaches up to polycrystalline silicon through the (platinum, ruthenium, etc.) layers, preventing the (conventional structure 6) from solving the conventional technology problems, including the one that an insulating layer is formed by oxidation.

10       Such conventional technology problems also occur not only from the specific materials described above, but also from layers consisting of (platinum, ruthenium, etc.) classified into noble metals, layers consisting of (Ti, Ta, TiN, etc.) classified into an anti-diffusion non-oxide conductive layer, and a ruthenium oxide layer classified into a conductive oxide even when those materials are classified according to more general categories. In other words, both (conventional  
15       structure 4) and (conventional structure 6) are represented using more general material categories, that is, oxide dielectric/noble metal/anti-diffusion non-oxide dielectric layer/polycrystalline silicon in the (conventional structure  
20       7) and oxide dielectric/conductor oxide/noble metal/polycrystalline silicon in the (conventional structure 8). The  
25       problems caused by each of the above layers which make up the above-described capacitor are summarized as follows.

At first, a noble metal layer will cause the following problems. (a) A noble metal layer will possibly cause a high resistance silicide to be formed if it comes in contact with silicon. (b) A noble metal layer will possibly become a diffusion path between chemical elements composing silicon, oxygen, and oxide. The problems which arise from oxide dielectric and conductive oxide layers will be as follows. (c) Such a layer will possibly oxidize the electrodes, thereby increasing the electrode resistance or insulating electrodes. Finally, an anti-diffusion non-oxide conductive layer will cause the following problem. (d) The layer will possibly be oxidized and its resistance will increase significantly.

If the characteristics of both (conventional structure 7) and (conventional structure 8) are considered here, the (conventional structure 9) will be considered based on an analogy of them. The (conventional structure 9) is obtained by compounding both of the structures simply. (Conventional Structure 9; oxide dielectric/conductive oxide/noble metal/anti-diffusion non-oxide conductive layer/polycrystalline silicon)

In this case, if an anti-diffusion non-oxide conductive layer is inserted, it is possible to solve one of the problems a) (silicidation) and (b) (the diffusion of chemical elements composing silicon and oxides). However, the above problems (b), (c), and (d) related to oxygen diffusion and oxidation of electrodes remain unsolved just like the (conventional structure 4), since the conventional indispensable conditions

for forming oxides in an oxidizing atmosphere are not improved at all.

In other words, the conventional technology cannot solve the problems such as oxygen diffusion and oxidation both caused by such oxides as oxide dielectrics and conductive oxides against such non-oxides as noble metals, anti-diffusion non-oxide conductive layers and polycrystalline silicon, not only when an oxide comes in contact with polycrystalline silicon directly, but also when an oxide comes in contact with polycrystalline silicon via a noble metal, as well as when an oxide comes in contact with an anti-diffusion non-oxide conductive layer via a noble metal.

As described above, in order to connect an oxide dielectric material to polycrystalline silicon electrically, an anti-oxidation layer must be formed between them. Conventionally, there has been no effective anti-oxidation layer. Instead of such a layer, therefore, a metallic layer consisting of platinum, etc. has been formed between them. Unfortunately, oxygen diffuses even at grain boundaries of such a metallic layer, thereby reaching the anti-oxidation layer and probably resulting in oxidation of the layer. The thickness of the metallic layer was increased in some cases to compensate for this disadvantage, but this resulted in an increase of the aspect ratio of the capacitor. This method will thus be undesirable for forming fine-structured memory cells. To solve this problem, therefore, a new and effective anti-diffusion or anti-oxidation layer has been awaited.

Under such circumstances, it is a first object of the present invention to provide a semiconductor device, which can solve the above conventional technology problems. In order to achieve the first object, the semiconductor device of the present invention is provided with a fine-structured memory, which can be highly integrated using an oxide dielectric material (including ferroelectrics) for the insulator of the capacitor.

It is a second object of the present invention to provide a method of manufacturing such a semiconductor device.

In order to solve the above problems, the semiconductor device of the present invention, which includes a capacitor consisting of an oxide dielectric layer formed on the top material, connects a semiconductor surface of a semiconductor substrate or on a substrate to an oxide dielectric material via at least two layer areas, each of which consists of a conductive material different from the other. The materials of these two conductor areas (or material compositions) are combined thereby suppressing an increase of the electric resistance generated in the conventional technology in the anti-diffusion or anti-oxidation layer disposed between a semiconductor area and an oxide dielectric material area.

The semiconductor device of the present invention comprises a first area consisting of a semiconductor material which is conductive (wiring layers and electrodes consisting of a semiconductor substrate or a semiconductor film); a second area connected to the first area and

consisting of a first conductive material; a third area  
connected to the second area and consisting of a second  
conductive material; a fourth area connected to the third  
area and consisting of an oxide dielectric material; and a  
5 fifth area connected to the fourth area and consisting of  
a conductive material. Thus, the semiconductor device of  
the present invention has characteristics as follows in terms  
of the basic configuration; that is, the material composition  
at the interface adjacent to the second area in the first area  
is approximately equal to the average material composition of  
the first area, and the material composition at the interface  
adjacent to the first area in the second area, as well as the  
material composition at the interface adjacent to the third  
area in the second area are approximately equal to the average  
material composition of the second area, respectively. As  
understood from these characteristics, the third and fifth  
areas form a capacitor via the fourth area. The oxide  
dielectric material which forms the fourth area may be  
replaced with a so-called ferroelectric material indicating a  
20 characteristic (hysteresis) that a polarization value is  
changed differently between increasing and decreasing an  
applied electrical field.

The present invention is characterized mainly as follows:  
The semiconductor is composed so that the first area has a  
25 material composition, which is approximately equal to the  
composition of the semiconductor material which forms the  
first area at the interface adjacent to the second area, and

so that the second area has a material composition, which is approximately equal to the composition of the first conductive material at the interface adjacent to the first area and to the third area. In other words, the semiconductor device of the present invention is composed so as to make the material composition approximately homogeneous within the first and second areas, respectively. And, there is no material (silicon oxide, metallic silicide, titanium oxide, etc. described above) that increases the electrical resistance in those areas. The materials that increase the electrical resistance as described above or the materials having an electrical insulating property actually (hereunder, to be referred to as a high resistance material) are formed around each interface between areas in a process in which the second to fourth areas are multi-stacked sequentially on the first area. On the contrary, according to the semiconductor device of the present invention, the first and second conductive materials are selected properly so as to prevent the formation of a high-resistance material at the interface between the first and second areas, as well as at the interface between the second and third areas; and further, the first area is formed so that its material composition at the interface adjacent to the second areas becomes approximately equal to the average material composition in the first area, and the second area is formed so that its material composition at the interface adjacent to the first area, as well as at the interface adjacent to the third area become approximately equal to the

average material composition in the second area. It will thus be understood clearly here that no high resistance materials are formed at the interface between the third and fourth areas because of the use of a noble metal of the (conventional structure 7) or the use of a conductive oxide of the (conventional structure 8) in the third area. In addition, an area (layer) consisting of a conductive material composed differently from the first and second conductive materials may be formed between the third and fourth areas; thereby, to improve the electrical conductivity needed between the first and third areas or improve the conditions for forming an oxide in the fourth area. In terms of the same aspect, an area (layer) consisting of a conductive material composed differently from the first and second conductive materials may be formed between the first and second areas. In short, what is important is that the second and third areas are connected to each other.

In an embodiment of the present invention, it is most important that the first and second conductive materials should be selected properly. There are two guidelines for selecting conductive materials. The object of the first guideline is as follows; two conductive materials are conductive oxides composed of the same chemical element and of the same framework of the crystal structure. The composition ratio of oxygen in the first conductive material is set lower than that in the second conductive material. In other words, the first conductive material is driven into an oxygen



deficiency state. The object of the second guideline is as follows; aluminum titanium nitride (TiAlN) is used as the first conductive material and an anti-oxidation metallic material is used as the second conductive material. In any of the guidelines, the two conductive materials should preferably be selected from those materials having a resistivity which is 10 mΩm (0.01 Ωcm) or under respectively. Hereunder, the present invention will be described in detail with reference to each of the guidelines. In the following description, the first to third areas (including a conductive material layer if it is provided between the third and fourth areas) will be referred to as the lower electrode and the fifth area as the upper electrode.

#### 1. Guideline 1 for selecting conductive materials

This guideline is directed to formation of the second and third areas used as a double-layered conductive oxide layer, which can suppress oxygen diffusion and oxidation (the third object of the present invention) in order to achieve the first object of the present invention, as well as to provide a method of manufacturing the double-layered conductive oxide layer, which can suppress oxygen diffusion and oxidation (the fourth object of the present invention) to achieve the second object of the present invention.

Here, description will be made first concerning the structure of a semiconductor device that uses a capacitor consisting of an oxide dielectric material, especially the structure of a semiconductor device composed of a double-

layered conductive oxide layer, etc. including a conductive oxide layer with oxygen deficiency. Next, description will be made sequentially concerning the characteristics and concrete examples of metallic layers, the characteristics, and concrete examples of anti-diffusion non-oxide conductive layers, and concrete examples of oxide dielectric materials. Description will also be made concerning the characteristics and concrete examples of double-layered conductive oxide layers including a conductive oxide layer with oxygen deficiency, respectively, together with means for achieving the second object of the present invention described above, that is, a method of manufacturing a semiconductor device of the present invention. The method for achieving the third object of the present invention will also be described in detail, together with the method for achieving the first and second objects. The method for achieving the fourth object of the present invention will be described in detail, together with the method for achieving the second object.

Next, description will be made concerning a semiconductor device that will achieve the first object of the present invention described above. The semiconductor device of the present invention includes a capacitor composed of oxide dielectrics used as an insulator. Fig. 1 shows a schematic diagram of such a capacitor composed of oxide dielectrics. Fig. 1 does not show a detailed structure of the capacitor of the semiconductor device, which is composed of oxide dielectrics. It shows multi-stacked layers of the capacitor in

order to simplify the structure. An oxide dielectric capacitor consists of a lower electrode layer 11 formed on a substrate (shown only in the direction of the substrate side 10 in Fig. 1), an oxide dielectric layer 16 formed on the layer 11, and an upper electrode layer 17 formed on the layer 16. The lower electrode layer 11 includes a conductive oxide layer 12 and this conductive oxide layer 12 consists of two adjacent layers 14 and 15, which have the same crystal structure and consist of the same chemical elements. Each of the layers 14 and 15 has a composition ratio of oxygen different from the other. In other words, only the conductive oxide layer 14 positioned at the substrate side has an oxygen deficiency. These conductive oxide layers 14 and 15 correspond to the second and third areas described above.

In such a semiconductor device, the lower electrode layer 11 is connected electrically to the source area or the drain area of a MOS transistor formed on the substrate via the lower electrode layer component 13 including at least more than one layer formed closer to the substrate than the conductive oxide layer 14 with oxygen deficiency. Hereunder, an example of this lower electrode layer component 13 will be described in detail with reference to Figs. 2, 3 and 4.

Fig. 2 shows a configuration of an oxide dielectric capacitor when the lower electrode layer component 13 which is positioned closer to the substrate than the conductive oxide layer 14 with oxygen deficiency in Fig. 1 consists of a conductive polycrystalline silicon layer 20. The conductive

polycrystalline silicon layer 20 mentioned here corresponds to the first area described above. A structure in which an oxide comes in contact with silicon directly is not favorable as described above with respect to the conventional structure, since silicon is oxidized unavoidably under typically necessary conditions for crystallizing the oxide, that is, at 500°C or higher in an oxidizing atmosphere. According to the present invention, however, the conductive oxide layer 14 with oxygen deficiency is formed adjacent to the polycrystalline silicon layer 20, so that the structure as shown in Fig. 2 is realized. The characteristics of the double-layered conductive oxide layer 12 including the conductive oxide layer 14 with oxygen deficiency will be described later.

Fig. 3 shows the configuration of an oxide dielectric capacitor when the component 13 forming the lower electrode layer consists of a non-oxide conductive layer for anti-diffusion 30 and a conductive polycrystalline silicon layer 20. The lower electrode layer is positioned closer to the substrate side than the conductive oxide material 14 with oxygen deficiency as shown in Fig. 1. The anti-diffusion non-oxide conductive layer 30 corresponds to a layer formed between the first and second areas described above. The conventional technologies cannot avoid oxidization of the anti-diffusion non-oxide conductive layer caused by the oxygen that diffuses at grain boundaries in a noble metal at 500°C or over in an oxidizing atmosphere, even when a noble metal is used to separate the oxide from the anti-diffusion non-oxide

conductive layer as seen in the (conventional structure 7). Those are typical conditions needed to crystallize an oxide. Thus, such a structure which places an oxide in contact directly with the anti-diffusion non-oxide conductive layer 30 as described above is not suitable. According to the present invention, however, when a conductive oxide layer 14 with oxygen deficiency is positioned adjacent to the anti-diffusion non-oxide conductive layer 30, the structure as shown in Fig. 3 is realized. The characteristics of the double-layered conductive oxide layer 12 including the conductive oxide layer 14 with oxygen deficiency will be described later.

Fig. 4 shows the configuration of an oxide dielectric capacitor when the component 13 forming the lower electrode layer positioned closer to the substrate side than the conductive oxide material 14 with oxygen deficiency shown in Fig. 1 consists of a metallic layer 40, an anti-diffusion non-oxide conductive layer 30, and a conductive polycrystalline silicon layer 20. The metallic layer 40 and the anti-diffusion non-oxide conductive layer 30 correspond to a layer formed between the first and second areas described above. The conventional technologies cannot avoid oxidization of the anti-diffusion non-oxide conductive layer, which is caused by oxygen diffusion through the metallic layer 40 at 500°C or higher in an oxidizing atmosphere, which are typical conditions needed to crystallize oxides. In order to suppress such oxidization, therefore, the thickness of the metallic layer 40 must be increased as described above. According to

the present invention, however, a conductive oxide layer 14 with oxygen deficiency is positioned adjacent to the metallic layer 40. The structure as shown in Fig. 4 is thus realized regardless of how thin the metallic layer 40 is. The characteristics of the double-layered conductive oxide layer 12 including the conductive oxide layer 14 with oxygen deficiency will be described later.

A noble metal highly resistant to oxidization will be considered as a candidate for forming such a metallic layer. Concretely, among noble metals, at least one of the following noble metal elements will be suitable; platinum which is highly resistant to oxidization, ruthenium, or iridium composed of the same element as the noble metal element included in the conductive oxide layer to be described later.

Hereunder, materials suitable for the anti-diffusion non-oxide conductive layer will be described. Necessary conditions to satisfy the requirements of the anti-diffusion non-oxide conductive layer 30 are conductivity at first, then resistance to oxidization, and resistance to reaction with silicon. Compounds to be considered as candidates for the anti-diffusion non-oxide conductive layer 30 are nitride, silicide, boride, and carbide. The anti-reaction to silicon is stable in any of those compounds. Any of them can be used with no problem. Of course, if the object semiconductor device is annealed at 1000°C or higher, the elements of any of those compounds will react to silicon, thereby forming reaction products of high resistance or insulation properties possibly.

However, a back-end process including the formation of an oxide dielectric capacitor for a semiconductor device will require only a heating condition of 800° at the highest for a few minutes, which will not form such reaction products caused by mutual diffusion of elements. The reaction to silicon can thus be neglected. As for the resistance to oxidization, there will arise no problem in the case where the conductive oxide layer with oxygen deficiency of the double-layered conductive oxide layer is put adjacent to the anti-diffusion non-oxide conductive layer (Fig. 3). As will be described later, this is because the conductive oxide layer with oxygen deficiency must be formed in a non-oxidizing atmosphere and the conductive oxide layer with oxygen deficiency functions as an obstacle in the oxygen diffusion path. In addition, since the conductive oxide layer with oxygen deficiency is over-stacked on the anti-diffusion non-oxide conductive layer 30 with a metallic layer therebetween (Fig. 4), the anti-diffusion non-oxide conductive layer 30 is separated farther from the oxide layer. In addition, forming a metallic layer adjacent to the anti-diffusion non-oxide conductive layer has never caused any problem conventionally.

Hereunder, a concrete example of the anti-diffusion non-oxide conductive layer will be described. A nitride will be suitable if it includes at least one of such metal types as Ti, Ta, Zr, Nb, V, and W, since it becomes very conductive. In addition to those materials, a silicide such as Ti, a boride such as La, and a carbide such as Ti, will also

be suitable.

Next, materials suitable for an oxide dielectric layer will be described. Ferroelectric materials are also oxide dielectric materials, of course. There is no reason to limit the materials. There are some well-known materials as shown below, however. Typical examples of oxide dielectrics of which the center element is titanium are; lead zirconate titanate obtained by replacing part or all of the titanium with zirconium, lead barium zirconate titanate obtained by replacing part or whole of the lead with barium, and barium strontium titanate including only alkaline earth metals, etc. As typical examples of bismuth-system dielectrics composed in a layered structure, there are bismuth layered dielectrics such as  $\text{Bi}_4\text{Ti}_3\text{O}_{12}$ ,  $\text{SrBi}_2\text{Ta}_2\text{O}_9$ , etc.

In addition to those well-known oxide dielectrics and oxide ferroelectrics, new oxide dielectrics and oxide ferroelectrics to be discovered in the future, etc. are usable as the oxide dielectric layer described above.

Next, the characteristics of the double-layered conductive oxide layer 12 including a conductive oxide layer with oxygen deficiency will be described, as mentioned in the description of the structures shown in Figs. 2 to 4. Here, description will be made for the structure, function, and manufacturing method of the double-layered conductive oxide layer in order to achieve the method of manufacturing the semiconductor device, which is the second object of the present invention, the function of the double-layered



conductive oxide layer that can suppress oxygen diffusion and oxidation, which is the third object of the present invention, and the method of manufacturing the double-layered conductive oxide layer, which is the fourth object of the present invention.

As described above, it is the oxidizing of the anti-diffusion non-oxide conductive layer and polycrystalline silicon that are already stacked that creates a problem when forming an oxide layer for dielectrics and electrodes. The oxidation is caused by an oxidizing atmosphere, which is indispensable for forming oxide layers. What must be emphasized here is that the problem is not due to a reaction between oxide and silicon or between oxide and an anti-diffusion non-oxide conductive layer. In terms of the standard Gibbs free energy, oxides composed of alkali earthmetals such as Sr and Ca, and transition elements such as Ru and Ti are more stable than oxidation of Si. An anti-diffusion non-oxide conductive layer composed of nitride, silicide, boride, and carbide of transition metals cannot be expected to be oxidized through reaction with an oxide in terms of the free energy. If anything, they are all oxidized by an oxidizing active gas in the atmosphere needed for forming an oxide layer. Consequently, the present inventor has concluded that the above problems can be solved if an oxide layer is formed in a non-oxidizing atmosphere in expectation that the other elements which make up the semiconductor device of the present invention would not be oxidized.

Generally, the oxide dielectrics (including ferroelectrics) forming an oxide dielectric-capacitor and oxide films such as conductive oxide electrodes are formed in an oxidizing atmosphere. This is mainly because oxides are unstable chemically in a non-oxidizing atmosphere and no oxide film is formed or even when it is formed, its characteristics are not satisfactory. Because the vapor pressure of typical elements is high, film formation under an insufficient oxidizing condition surely causes selective evaporation, that is, a variation in composition in oxide ferroelectrics including group-4 and group-5 typical elements such as lead and bismuth. At the same time, since decomposed products other than object compounds also come to be mixed, the ferroelectric properties are degraded significantly. In addition, the non-oxidizing atmosphere causes oxygen deficiency in the object compound. In the case of oxide dielectrics including group-4 transition elements such as titanium and zirconium, oxygen deficiency will cause the dielectric constant to be lowered, which causes a leakage current to flow. Consequently, it is not realistic to form an oxide dielectric film in a non-oxidizing atmosphere.

As for another oxide for forming oxide dielectric capacitors, that is, conductive oxide electrodes, it was expected that films could be formed in a non-oxidizing atmosphere as long as this does not affect the characteristics of electrodes or the object semiconductor device even when oxygen deficiency was introduced into compounds and

simultaneously decomposed products were mixed while the films were formed in a non-oxidizing atmosphere. In other words, the oxygen deficiency reduces or increases the charge density, as well as changes its mobility, thereby increasing its resistivity. However, no problem arises as long as the resistivity required for the electrode layer is secured. Forming films in a non-oxidizing atmosphere will also create no problem as long as the resistance required for the electrode layer is secured even when the resistivity is increased by coexistence of some decomposed products.

The component 13 of the lower electrode layer adjacent to the conductive oxide layer 12 in Fig. 1, corresponds to the polycrystalline silicon layer 20 in Fig. 2, the anti-diffusion non-oxide conductive layer 30 in Fig. 3, and the anti-diffusion non-oxide conductive layer 30 through the metallic layer 40 in Fig. 4, respectively. In order to prevent those layers from oxidizing, the present inventor thought it would be better to form the side 14 at which the conductive oxide layer 12 was adjacent to the component 13 (20, 30 and 40) of the lower electrode layer in a non-oxidizing atmosphere. The layer 14 was thus formed up to a certain thickness. And, the rest of the layer 15 of the conductive oxide layer 12 was formed continuously in an oxidizing atmosphere by changing the oxidizing activity of only the film deposition conditions, such as the oxygen pressure and the type of the oxidizing gas. In other words, the conductive oxide layer 12 is composed of two adjacent

layers 14 and 15, and these two layers are formed to have the same crystal structure and of the same element, but differently from each other in the composition ratio of oxygen. Only the layer 14 of the two adjacent layers includes an oxygen deficiency. The layer 14 is positioned at the component 13 side of the lower electrode layer, that is, at the substrate side.

Since the conductive oxide layer 14 is formed in a non-oxidizing atmosphere, the adjacent lower electrode layer component 13 (polycrystalline silicon layer 20, the anti-diffusion non-oxide conductive layer 30, and the metallic layer 40) is not oxidized. The conductive oxide layer 14 with oxygen deficiency, after it is formed once, is stable in terms of the standard Gibbs free energy. Then, the component 13 (20, 30, and 40) of the lower electrode layer is also not oxidized. And, as shown in Fig. 4, even when a metallic layer 40 is inserted therebetween, the anti-diffusion non-oxide conductive layer 30 is never oxidized by oxygen diffusion, so that the thickness can be reduced as much as possible.

After the formation of the conductive oxide layer 14 with oxygen deficiency, the conductive oxide layer 15 and the oxide dielectric layer 16 are formed in an oxidizing atmosphere. If the conductive oxide layer 14 includes an oxygen deficiency, the layer 14 acts as a diffusion buffer layer against oxygen even when those layers 15 and 16 are formed in an oxidizing atmosphere. In other words, even when

the surface of the conductive oxide layer 14 with oxygen deficiency is exposed to an oxidizing gas, the layer 14 acts as a buffer layer against the oxygen diffusion ions, and captures diffusing oxygen ions as well. Since the conductive oxide layer 14 itself is stable in terms of the standard Gibbs free energy, the layer 14 acts as an anti-oxidation layer for the component 13 (20, 30, and 40) of the lower electrode layer.

Consequently, the double-layered conductive oxide layer including a conductive oxide layer with oxygen deficiency, which is formed in a non-oxidizing atmosphere, acts as an excellent oxidation resistant film and an oxygen diffusion barrier layer.

The thickness of the conductive oxide layer 14 (with oxygen deficiency), which is formed in a non-oxidizing atmosphere, should preferably be 10nm or larger. The reason is that the component 13 (20, 30, and 40) of the lower electrode layer is completely covered so as to be prevented from oxidizing when the conductive oxide layer 15 and the oxide dielectric layer 16 are formed in an oxidizing atmosphere. The upper limit is not determined specially for the thickness. All of the conductive oxide layers 12 may be composed of a conductive oxide layer 14 (with oxygen deficiency) which is formed in a non-oxidizing atmosphere.

In this case, however, since the following oxide dielectric layer 16 is formed off course in an oxidizing atmosphere, the interface of conductive oxide layer 14 adjacent to the

oxide dielectric layer 16 is oxidized. Consequently, a thin layer 15 is formed at the interface. The double-layered conductive oxide layer 12 can thus be formed.

Hereunder, a non-oxidizing atmosphere will be described with respect to a method for manufacturing the double-layered conductive oxide layer. A one type of non-oxidizing atmosphere is an atmosphere including a hydrogen gas and a reducing gas. In such a reducing atmosphere, however, much oxygen is taken out while an oxide film is grown in the film deposition process. The film is thus possibly reduced to a metal. A milder non-oxidizing atmosphere is an inactive gas atmosphere that uses inert gases such as argon and helium, or a vacuum into which none of oxidizing gases such as oxygen ( $O_2$ ), nitride monoxide ( $N_2O$ ), nitric dioxide ( $NO_2$ ), ozone ( $O_3$ ), etc. is introduced intentionally. If the component 13 of the lower electrode layer is assumed to be an anti-diffusion non-oxide conductive layer 30 (or a metallic layer 40) and a conductive oxide layer to be formed is more reactive to oxygen than the anti-diffusion non-oxide conductive layer 30, it can apply a weak oxidizing atmosphere including oxidizing gases such as oxygen, nitrogen monoxide, nitrogen dioxide and ozone, etc. slightly. In other words, as described in the conventional technologies, there is a greater possibility that the anti-diffusion non-oxide conductive layer is oxidized in a remarkable oxidizing atmosphere. In the atmosphere including a slight oxidizing gas, the anti-diffusion non-oxide conductive layer is not oxidized while a conductive oxide layer with

oxygen deficiency can be formed. This is because an energy barrier for oxidation exists between the anti-diffusion non-oxide conductive layer in which compounds are already formed and the conductive oxide layer.

5           Concretely, the condition of a non-oxidizing atmosphere depends on respective film deposition methods with which a conductive oxide layer is formed. At first, when an oxide film is formed in an inert gas or inactive gas atmosphere or in a vacuum, no oxygen is supplied from the growth environment. The  
10 film deposition source must include oxygen. This film deposition category includes a sputtering method, a laser deposition method, both of which use a sintered oxide target, an electron beam evaporation method that uses an oxide evaporation source, etc. Since the sputtering method needs a  
15 discharge gas, introduction of argon (Ar) gas of 3N (99.9%) or up in purity by a few mTorr to a few tens of mTorr will do. It should be avoided, however, to use a gas of low purity, since such a gas brings about an unexpected result such as unstable discharge, precipitation of impurity phases, etc. The laser  
20 deposition method can form oxide films in a vacuum. Of course, no problem will occur if any of the inert gases are used just like in the sputtering method, but it makes no sense principally. Films can also be formed by an electron beam deposition method that uses an oxide evaporation source. The  
25 vacuum mentioned here is a state achieved by any of the known evacuation devices without introducing oxidizing gases such as oxygen, nitrogen monoxide, nitrogen dioxide, ozone, etc.

intentionally. The pressure should preferably be  $1\mu\text{Torr}$  or under in terms of the non-oxidizing atmosphere in both laser deposition and electron beam deposition methods.

Each of the film deposition methods described above can be applied to form an oxide film on the anti-diffusion non-oxide conductive layer (including a case when the layer is formed via a metallic layer) in a weak oxidizing atmosphere including oxidizing gases such as oxygen, nitrogen monoxide, nitrogen dioxide, ozone, etc. slightly. The sputtering method is just required to include an oxidizing gas used as a discharge gas. The laser deposition method is just required to include an oxidizing gas. The electron beam deposition method, when used in a vacuum, can use only an oxide as an evaporation source. When it is used in a weak oxidizing atmosphere, however, it can also use a metal evaporation source. Consequently, the method can use a heater such as an effusion cell (K cell) as a heating source in addition to the electron beam. The pressure should preferably be  $10\mu\text{torr}$  or lower in total pressure or partial pressure of the oxidizing gas in use in terms of the non-oxidizing atmosphere in any of the sputtering method, the laser deposition method, and other deposition methods that use an electron beam and a heater.

On the basis of the ideas described above, the following results have been obtained when checking the conductive oxides that can satisfy the conditions with respect to the rutile structure, the perovskite structure, and the  $\text{ReO}_3$  structure in which many conductive oxides are



known: (a) The resistivity in the room temperature is 0.01  $\Omega$ cm or lower. (b) Possible to be stabilized in a non-oxidizing atmosphere and under typical conditions (oxygen pressure of 1  $\mu$ Torr and temperature of 700°C.

5 In order to satisfy the above requirement (b), it is not desirable that a conductive oxide is composed of a multi-valent ion, such as a positive center cation. Consequently, conductive oxides including Cr, Mn, Fe, Co, Ni, Cu, and V are excluded.

10 There are two conductive oxides that crystallized in the rutile structure;  $\text{RuO}_2$  and  $\text{IrO}_2$ .

15 There are three conductive oxides that crystallized in the perovskite structure:  $\text{CaRuO}_3$  and  $\text{SrRuO}_3$ , whose center element is Ru (ruthenium), and (La, Sr)  $\text{TiO}_3$ , in which part of Sr of  $\text{SrTiO}_3$ , whose center element is Ti (Titanium) is replaced with La by over 0.5 weight % to 4.0 weight % (included) in quantity.

$\text{ReO}_3$  is another conductive oxide that takes the  $\text{ReO}_3$  structure.

20 When forming a conductive oxide in a non-oxidizing atmosphere, oxygen deficiency is introduced as described above. In the thermal equilibrium state, only a slight oxygen deficiency of 0.1% or lower is introduced as a point defect, but film deposition is often carried out in a non-equilibrium  
25 state. Thus, an extra oxygen defect is easily frozen excessively unlike in the thermal equilibrium state. It is very difficult, however, even with the current analysis

technique to measure an oxygen defect concentration specific to films. Actually, it is impossible to define an oxygen defect concentration with an accurate value. On the other hand, no remarkable impurity was identified when a crystal structure of the film which was deposited in a non-oxidizing atmosphere was analyzed by an X-ray diffractometer. The stoichiometry of cations could be confirmed in the compositional analysis using the ICPS (inductivity-coupled Plasma Spectroscopy). At this time, the resistivity increased by almost 10% in maximum compared to deposition of the same films in an oxidizing atmosphere. This suggests that an oxygen deficiency is surely introduced.

A film formed in a non-oxidizing atmosphere will be defined concretely as follows on a condition that the permissible oxygen deficiency allows an objective structure to be kept stable. For the rutile structure, it is defined that an oxygen deficiency  $x$  is larger than 0 and smaller than a value that enables the rutile structure to be kept stable in the chemical formula  $MO_{2-x}$  with oxygen deficiency in which both Ru and Ir transition elements are represented by M. For the perovskite structure, it is defined that the oxygen deficiency  $x$  is larger than 0 and smaller than a value (upper limit value) that enables the perovskite structure to be kept stable in the chemical formula  $AMO_{3-x}$  with oxygen deficiency in which both Ru and Ti transition elements are represented by M, and Ca, Sr, and La elements are represented by A, respectively. At this time, even when an anti-site

defect is introduced between cations due to the introduced oxygen deficiency, such that the lattice constant becomes larger than the standard bulk value, the basic framework is judged to be still within the category of the perovskite structure. For the  $\text{ReO}_3$  structure, it is defined that the oxygen deficiency  $x$  is larger than 0 and smaller than a value that enables the  $\text{ReO}_3$  structure to be kept stable in the chemical formula  $\text{MO}_{3-x}$  with oxygen deficiency.

The introduction of oxygen deficiency causes the resistivity of the conductive oxide to be increased by almost 10% in maximum, but the conductive oxide is kept low in resistivity sufficient to be used as electrodes. For example, the resistivity was increased by almost 10% in  $\text{SrRuO}_{3-x}$ , but the resistivity was as small as a few m $\Omega\text{cm}$  as an absolute value. In  $\text{IrO}_{2-x}$ ,  $\text{RuO}_{2-x}$ , and  $\text{ReO}_{3-x}$ , the resistivity was increased only to about double in maximum. In other words, it was confirmed that the conductive oxides could keep a resistivity sufficient to be used for electrodes even when the conductive oxides described above were formed in a non-oxidizing atmosphere.

A possibility of coexistence of decomposed products was as described above when a conductive oxide was formed in a non-oxidizing atmosphere. Both  $\text{RuO}_2$  and  $\text{IrO}_2$  in rutile structures, as well as the  $\text{ReO}_3$  are a monoxide respectively and each of those structures includes only one type of transition element. There is thus no fear that they are decomposed thereby to produce other compounds. On the other hand, the

perovskite structure expressed by  $\text{AMO}_3$  is a complex oxide which consists of an element M consisting of transition elements and an element A consisting mainly of alkaline-earth metals. It is thus possible that decomposed products coexist at a high temperature of about  $700^\circ\text{C}$  in a non-oxidizing atmosphere. Actually, when Ca was included as an alkaline-earth metal, it was confirmed by an X-ray diffractometer that about a few %  $\text{CaO}$  existed as a decomposed product. Even when Sr was included,  $\text{SrO}$  was observed as a decomposed product in a stronger non-oxidizing atmosphere, that is, at a higher temperature and at a lower pressure. In any of the cases described above, therefore, it was recognized that nothing affected the resistivity at room temperature. It was concluded from this result that highly resistant decomposed products were distributed and coexisted in a conductive oxide, so that a current was caused to flow in a lower objective conductive oxide.

At a lower temperature than room temperature, a metallic conduction was observed, where the resistivity was decreased as the temperature was decreased if there was no decomposed product. If decomposed products coexisted, a conduction that caused the resistivity to be increased, was observed. It was concluded from this result that the increase of the resistivity was caused by the conduction characteristics of decomposed products segregated along grain boundaries in a microscopic fashion.

In any of the cases described above, at the room

temperature or above, the increase of the resistivity caused  
by  
coexistence of decomposed products was within an allowable  
range for conductive oxide layers or semiconductor devices  
that used conductive oxide layers. In other words, each of the  
conductive oxides that take the perovskite structure may be a  
mixed phase of  $\text{CaRuO}_3$ ,  $\text{SrRuO}_3$ , and  $(\text{La}, \text{Sr}) \text{TiO}_3$  in which a  
part of Sr of  $\text{SrTiO}_3$  is replaced with La by over 0.5 to 4.0  
weight% (included), and an alkaline earthmetal oxide  $\text{CaO}$   
or  $\text{SrO}$  composing the subject oxide.

Description has been made so far of a means for  
achieving the first object of the present invention, that  
is the characteristics of a semiconductor device, using  
oxide dielectrics as a capacitor insulator and a double-  
layered conductive oxide layer as an electrode element, as  
well as for the means for achieving the second object of the  
present invention, that is, a method of forming the double-  
layered conductive oxide layer, selected from the methods of  
manufacturing such a semiconductor device, and for the means  
for achieving the third object of the present invention, that  
is, the characteristics of the double-layered conductive oxide  
layer that can suppress oxygen diffusion and oxidation, and  
for the means for achieving the fourth object of the present  
invention, that is, a method of forming the double-layered  
conductive oxide layer.

Finally, description will be made of means for achieving  
the second object of the present invention, that is, a method

of manufacturing such a semiconductor device. The method of manufacturing the semiconductor device of the present invention includes processes for forming a lower electrode layer on a substrate as described above with reference to Figs. 1 to 4. The lower electrode layer consists of a polycrystalline silicon layer, a non-oxide conductive layer for anti-diffusion, a metallic layer, and a double-layered conductive oxide layer. Usually, a polycrystalline silicon layer is formed using chemical vapor deposition. The non-oxide conductive layer for anti-diffusion is formed using a sputtering method, a vacuum deposition method, and a CVD method. The metallic layer is formed using a sputtering method. However, the methods for forming those layers are just examples and they are not limited for modification specially. How to form the double-layered conductive oxide layer is as described above in detail. The compound of each layer for composing the lower electrode is also as described above in detail.

In order to form an oxide dielectric capacitor in which an oxide dielectric layer is positioned between the upper and lower electrode layers, an oxide dielectric layer is formed on this lower electrode layer, then the upper electrode layer is formed on the oxide dielectric layer. Concrete compounds used for forming the oxide dielectric layer are as described above in detail. The sol-gel method with use of alkoxide, the vacuum deposition method, the chemical vapor deposition method, the sputtering method, etc. can be used to form the

oxide dielectric layer. The methods are not limited only to those specially identified. The upper electrode layer should preferably be formed with the same conductive oxide as that of the lower electrode layer if the symmetry of the current-voltage characteristics of the dielectric capacitor, as well as the symmetry of the polarization hysteresis curve of the ferroelectric capacitor are considered to be important. However, the semiconductor device will work as expected even if the conductive oxide and a noble metal such as platinum, ruthenium, and iridium are different between the upper and lower electrode layers. The upper electrode layer can be formed by any of sputtering, vacuum deposition, sol-gel, and chemical vapor deposition methods. The film deposition method is not limited only to those specially provided even when a noble metal is used for forming the upper electrode layer.

Before the oxide dielectric capacitor, that is, the lower electrode layer is formed, part of a MOS transistor is formed on the substrate. The source area or the drain area of the MOS transistor is connected electrically to the lower electrode layer through the conductive material filled in the contact holes formed through the insulator, which covers the semiconductor substrate on which the MOS transistor itself is formed. Polycrystalline silicon formed using the chemical vapor deposition method is often used as the conductive material filled in these contact holes. The polycrystalline silicon deposition method and the filling

material are not limited only those specially mentioned.

## 2. Guideline 2 for Selecting Conductive Materials

This guideline is determined to achieve the first and second objects of the present invention, especially on the basis of the configuration of (the conventional technology 7).

In order to achieve the first object of the present invention, the semiconductor device of the present invention is provided with oxide dielectric capacitors formed on a semiconductor substrate. The capacitor consists of a lower electrode layer including an aluminum titanium nitride layer, an oxide dielectric layer formed on the aluminum titanium nitride layer, and an upper electrode layer formed on the oxide dielectric layer. Figs. 5 and 6 show two typical cross sectional views of the lower electrode layer. Figs. 5 and 6 do not show any detailed structure of the oxide dielectric capacitor provided in the semiconductor device of the present invention, but they show simplified views of how each layer of the capacitor is stacked.

In Fig. 5, the lower electrode layer 11 consists of the aluminum titanium nitride layer 50 formed on the polycrystalline silicon layer 20, and the metallic layer 40 formed on the layer 50. The conductive polycrystalline silicon layer 20 corresponds to the first area described above in the concept of the semiconductor device. The aluminum titanium nitride layer 50 corresponds to the second area described above in the concept of the semiconductor device. The metallic



layer 40 corresponds to the third area described above in the concept of the semiconductor device. In Fig. 6, a conductive oxide layer 60 is stacked on the component of the lower electrode layer 11 shown in Fig. 5. This conductive oxide layer 60 corresponds to an area provided between the third and fourth areas described above in the concept of the semiconductor device.

The lower electrode layer 11 is also connected electrically to a predetermined area of the semiconductor element formed on the substrate, for example, the source or drain area of a MOS transistor.

Hereunder, the function of the aluminum titanium nitride layer 50 used for preventing oxygen diffusion and oxidation will be described. As provided in the conventional technologies, the titanium nitride layer used as a layer for preventing oxygen diffusion and oxidation, which has been examined so far, is weak in anti-reaction to oxygen. And, in order to compensate this weak point of the titanium nitride layer, it is indispensable to put a metallic layer made of platinum, etc. therebetween. A platinum layer of about 200nm in thickness is also needed to secure a time of oxygen diffusion at grain boundaries in the platinum. On the other hand, the titanium nitride layer still has an attraction, since it acts to prevent oxidization to a certain level while it keeps a high conductivity. This is why aluminum is added to titanium nitride to obtain a remarkable resistance to oxidization. The resistance was found as a result of

examination for the possibility of improvement of the resistance to oxidization by adding the second metallic element to titanium nitride.

10 The reaction of a nitride to oxidization, thereby to  
5 be changed into an oxide, is considered to be a reaction to substitute oxygen with nitrogen in the nitride. In other words, it may be considered that the height of the energy barrier between the nitride and the oxide dominates this substitution qualitatively. In the aluminum titanium nitride obtained by the present invention, the improvement of the anti-reaction to oxygen is considered to be caused by this heightened energy barrier. Regardless of this chemical background, however, it was found that the aluminum titanium nitride could function sufficiently as an anti-oxidizing layer if part of the titanium in the titanium nitride is replaced with aluminum. In terms of this anti-oxidizing property, if the chemical formula of the aluminum titanium nitride was expressed by  $(\text{Ti}_{1-x}\text{Al}_x)_{1-y}\text{N}_y$ , x should preferably be 0.2 or above and y should preferably be 0.4 or above. If x is smaller  
20 than 0.2, the anti-oxidizing property is not improved at all. If y is smaller than 0.4,  $\text{TiO}_2$  produced by oxidization is observed in an X-ray diffraction measurement.

Aluminum nitride is a high resistant material. If part of the titanium is replaced with aluminum, the resistivity  
25 increases. If such aluminum titanium is to be used for each electrode of a semiconductor device, the resistivity should preferably be 10mΩcm or under. Consequently, if aluminum

5 titanium nitride is represented by a chemical formula of  $Ti_{1-x}Al_x)_{1-y}N_y$ , x should preferably be 0.5 or below and y should preferably be between 0.4 and 0.6. If an impurity phase is precipitated, the material becomes non-homogeneous in the electrode, and thereby the forming of fine-integrated memory cells is disabled. In order to avoid this, the x value should preferably be 0.6 or below and the y value should preferably be 0.2 or above, and 0.6 or below.

10 In conclusion, the x value should preferably be 0.2 or above, and 0.5 or below and the y value should preferably be 0.4 or above, and 0.6 or below in the aluminum titanium nitride expressed by a chemical formula of  $Ti_{1-x}Al_x)_{1-y}N_y$ .

15 Another requirement for the aluminum titanium nitride layer, that is, the property of anti-diffusion is expected to be equivalent to that in the titanium nitride layer, since the structure of titanium nitride which is a mother compound is maintained, intrinsically. Thus, no problem is found specially from the layer.

20 The metallic layer 40 covering the aluminum titanium nitride layer shown in Figs. 5 and 6 should preferably be at least one of the noble metals which has excellent anti-oxidizing properties, that is, platinum, iridium, and ruthenium. For the conventional structure in which the anti-oxidizing layer is made of titanium nitride, the metallic  
25 layer had to be about 200nm in thickness. For the aluminum titanium nitride layer of the present invention, the resistance to oxidization is already improved. For example,

30nm will do as the thickness of the metallic layer as long as the layer can cover the surface of the aluminum titanium nitride layer completely.

For the structure shown in Fig. 5, an oxide dielectric layer 16 is formed on the metallic layer 40. However, a conductive oxide layer 60 may be inserted between the oxide dielectric layer 16 and the metallic layer 40 as a component of the lower electrode layer. The conditions for forming a conductive oxide layer in an oxidizing atmosphere are usually the same as those of forming an oxide dielectric layer. Thus, it may be considered that the resistance to oxidization required for the aluminum titanium nitride layer is also the same. Since such a conductive oxide layer can improve the contact property at each interface with a metallic layer, if it includes the same elements of a noble metal as those of the metallic layer, it should preferably be at least one of  $\text{IrO}_2$ ,  $\text{RuO}_2$ ,  $\text{SrRuO}_3$ , and  $\text{ReO}_3$ .

Hereunder, preferred materials for the oxide dielectric layer 16 will be described. There is no reason to limit the materials for the layer 16 specially. The following materials usable for the layer 16 are well known. Typical examples of oxide dielectrics whose center element is titanium are lead zirconate titanate obtained by replacing part or all of the titanium with zirconium, lead barium zirconate titanate obtained by replacing part or all of the lead with barium, barium strontium titanate including only alkalline-earth metal elements, etc. As typical examples of bismuth dielectrics with

a layered structure, there are bismuth layered dielectrics such as  $\text{Bi}_2\text{Ti}_2\text{O}_{12}$ ,  $\text{SrBi}_2\text{Ta}_2\text{O}_9$ , etc. In addition to those examples, other well-known oxide dielectrics, oxide ferroelectrics, and new oxide dielectrics and oxide ferroelectrics to be discovered in the future are all usable as the oxide dielectric layer described above.

The upper electrode layer 17 maybe any material if it is conductive. The materials are not limited only to metals and oxides. Each of the noble metals described above (in the example of the metallic layer 40 provided in the lower electrode layer) is usable. Each of the oxides described above (in the example of the conductive oxide layer 60 provided in the lower electrode layer) is usable. The materials of the upper electrode layer 17 are not limited only to those specially mentioned.

Next, description will be made of a method of manufacturing the semiconductor device of the present invention in order to achieve the second object described above. The method of manufacturing the semiconductor device of the present invention includes a process for forming the lower electrode layer including an anti-diffusion and anti-oxidation layer of aluminum titanium nitride which is formed in a nitriding atmosphere using the sputtering method. Various types of sputtering targets are usable; for example, a metallic target consisting of a titanium aluminum alloy, a composite-target obtained by putting an aluminum metal or aluminum nitride on a titanium target, a composite-target

obtained by putting a titanium metal or a titanium nitride on an aluminum target, a dual target consisting of a titanium target and an aluminum target and sputtered simultaneously, a nitride target consisting of an aluminum titanium nitride, a composite-target obtained by putting an aluminum metal or an aluminum nitride on a titanium nitride target, a composite-target obtained by putting a titanium metal or a titanium nitride on a aluminum nitride target, a dual target consisting of an aluminum nitride target and a titanium nitride target separately and so as to be sputtered simultaneously, may be employed. Any of DC and AC can be used for the sputtering discharge. If an aluminum nitride whose resistance is large is used as a target, however, an RF discharging is required.

At least, a discharge gas and a nitrogen gas must be included in the atmosphere used for forming an anti-diffusion and anti-oxidation layer of aluminum titanium nitride. An inert gas can be used as a discharge gas. However, usually an argon gas is used in consideration of economy. A nitrogen gas is included in the discharge gas by 10 to 90 mole%, since it requires sufficient nitridation and a high through-put (high deposition rate). If there is no restriction for both the semiconductor device and the environment, a few percent ammonia gas may be included thereby to accelerate nitridation and suppress oxidation.

The temperature should preferably be above room temperature to 600°C (included) when an aluminum titanium nitride anti-diffusion and an anti-oxidation layer are to

be formed with the sputtering method. Of course, room temperature does not mean that samples are kept in the room temperature, but it means that the samples should not be cooled or heated specially. Natural rising of the temperature should be allowed during the sputtering. When a sample was formed at a temperature above 600°C in a heating process, it was observed by an X-ray diffraction measurement that an aluminum nitride (AlN) was generated separately from the sample.

Furthermore, in order to achieve the second object described above, the method of manufacturing the semiconductor device of the present invention includes a process for completing the lower electrode layer by stacking a metal layer, or a metal layer and a conductive oxide layer sequentially on an anti-diffusion and anti-oxidation layer of aluminum titanium nitride. On this lower electrode layer, an oxide dielectric layer is formed. Then, the upper electrode layer is stacked thereon so that an oxide dielectric capacitor is formed in a structure so that the oxide dielectric layer is positioned between the upper and lower electrode layers. The metallic layer may be formed with any sputtering method, vacuum evaporation method, etc. As for the conductive oxide layer and the oxide dielectric layer, the sputtering method, the reactive evaporation method, the laser ablation method, the chemical vapor deposition method, the sol-gel method, etc. are usable. The method is not limited specially. The upper electrode layer may also be formed with any of those methods.

Before the oxide dielectric capacitor, that is, the lower electrode layer is formed, part of a MOS transistor is formed on the substrate. The lower electrode layer is connected electrically to the source area or the drain area of this MOS transistor through the conductive material filled in the contact holes perforated in the insulator, which covers the semiconductor substrate on which the MOS transistor itself is formed. Polycrystalline silicon formed using the chemical vapor deposition method is often used as the conductive material filled in these contact holes. The forming method and the filling material are not limited specially.

### 3. Characteristics of the Semiconductor Device of the Present Invention

The semiconductor device to be realized by an embodiment of the present invention on the basis of the above two guidelines for selecting conductive materials will have the following characteristics.

The semiconductor device of the present invention is provided with a first area (a semiconductor substrate or a semiconductor film, etc.) consisting of a conductive semiconductor material, a second area connected to the first area and consisting of the first conductive material, a third area connected to the second area and consisting of the second conductive material, a fourth area connected to the third area and consisting of an oxide dielectric, and a fifth area connected to the fourth area and consisting of a conductive material. And, the average resistivity of the first area is



almost equal to the resistivity of the semiconductor material  
composing the first area and the average resistivity of the  
second area is almost equal to the resistivity of the first  
conductive material composing the second area. Such  
5 characteristics mean that the respective electric resistances  
of the first to third areas are determined uniquely by the  
resistivity of the semiconductor material or the conductive  
material used for forming each of those areas, as well as by  
the length of the current path in each of those areas (or the  
10 thickness of each of those areas, if it is stacked  
vertically). In other words, the embodiment of the present  
invention can avoid the forming of a high resistant material  
almost completely in the first area or second area, which has  
been a problem of the conventional technology. And  
15 accordingly, it is possible to suppress an increase of the  
electrical resistance in those areas, as well as enabling the  
average resistivity in the current path from the first area to  
the third area to be set to 0.01  $\Omega\text{cm}$  or below.

Consequently, according to the present invention, when  
20 both the oxide dielectric layer and the conductive oxide layer  
are formed, memory cells can be formed without oxidizing the  
polycrystalline silicon layer adjacent to both the oxide  
dielectric layer and the conductive oxide layer, as well as  
the anti-diffusion non-oxide conductive layer consisting of a  
25 nitride, etc. Consequently, it becomes possible to reduce both  
the interfacial resistance and the contact resistance of each  
electrode, obtaining a semiconductor device provided with

fine-structured memory cells, suitable for high integration.  
In addition, the semiconductor device of the present invention  
can omit a process for forming a metallic layer of 200nm or  
over in thickness consisting of platinum and the like as an  
anti-oxidizing layer, and it can reduce the total thickness  
and the aspect ratio of the capacitor by thinning the lower  
electrode layer. It is thus possible for the present invention  
to obtain a semiconductor device provided with fined-  
structured memory cells to be formed through a fine-patterned  
process of the submicron region, for example, using gigabit  
class lithographic technology.

#### Brief Description of the Drawings

Fig. 1 is a diagram which illustrates an oxide dielectric  
capacitor provided with a double-layered conductive oxide  
layer included in its lower electrode layer.

Fig. 2 is a diagram which illustrates an oxide dielectric  
capacitor provided with a double-layered conductive oxide  
layer formed on a polycrystalline silicon layer.

Fig. 3 is a diagram which illustrates an oxide dielectric  
capacitor provided with a double-layered conductive oxide  
layer formed on an anti-diffusion non-oxide conductive layer.

Fig. 4 is a diagram which illustrates an oxide dielectric  
capacitor provided with a double-layered conductive oxide  
layer formed on an anti-diffusion non-oxide conductive layer  
through a metallic layer.

Fig. 5 is a diagram which illustrates an oxide dielectric  
capacitor provided with an oxide dielectric layer on a

metallic layer stacked on an aluminum titanium nitride layer.

Fig. 6 is a diagram which illustrates an oxide dielectric capacitor provided with an oxide dielectric layer on a conductive oxide layer stacked on an aluminum titanium nitride layer.

Figs. 7(a) and 7(b) are graphs which illustrate the electrical characteristics of the oxide dielectric capacitor formed so as to form a double-layered conductive oxide on a polycrystalline silicon layer. Fig. 7(a) illustrates the electrode resistance and Fig. 7(b) illustrates a polarization hysteresis curve.

Figs. 8(a), 8(b) and 8(c) are graphs which illustrate the electrical characteristics of the oxide dielectric capacitor formed so as to form a double-layered conductive oxide on a nitride layer. Fig. 8(a) illustrates the resistance of an electrode including a TiN layer and Fig. 8(b) illustrates the resistance of an electrode including a TaN layer and Fig. 8(c) illustrates a polarization hysteresis curve of a capacitor including a TiN layer.

Fig. 9 is a graph which illustrates a polarization hysteresis curve of an oxide dielectric capacitor formed so as to form a double-layered conductive oxide layer on a TiN layer through a metallic layer.

Figs. 10(a) and 10(b) are graphs which illustrate a compositional range of an aluminum titanium nitride. Fig. 10(a) indicates the x allowance in  $(\text{Ti}_{1-x}\text{Al}_x)_{0.5}\text{N}_{0.5}$ . Fig. 10(b) indicates the y allowance in  $(\text{Ti}_{0.6}\text{Al}_{0.4})_{1-y}\text{N}_y$ .

Fig. 11 is a graph which illustrates a polarization hysteresis curve of an oxide dielectric capacitor provided with an aluminum titanium nitride layer. Curve (a) indicates a case where an oxide dielectric layer stacked on a metallic layer and curve (b) indicates a case where an oxide dielectric layer is stacked on a conductive oxide layer.

Fig. 12 is a diagram which illustrates a manufacturing process of the semiconductor device of the present invention.

Fig. 13 is a diagram which illustrates a manufacturing process of the semiconductor device of the present invention.

Fig. 14 is a diagram which illustrates a manufacturing process of the semiconductor device of the present invention.

Fig. 15 is a diagram which illustrates manufacturing process of the semiconductor device of the present invention up to a planarizing process.

Fig. 16 is a diagram which illustrates a manufacturing process of the semiconductor device in which a double-layered conductive oxide layer is formed on a polycrystalline silicon layer.

Fig. 17 is a diagram which illustrates a manufacturing process of the semiconductor device in which a double-layered conductive oxide layer is formed on an anti-diffusion non-oxide conductive layer.

Fig. 18 is a diagram which illustrates a manufacturing process of the semiconductor device in which a double-layered conductive oxide layer is formed on an anti-diffusion non-oxide conductive layer through a metallic layer.

Fig. 19 is a diagram which illustrates a manufacturing process of the semiconductor device which is provided with an aluminum titanium nitride layer formed so as to form an oxide dielectric layer on a metallic layer.

Fig. 20 is a diagram which illustrates a manufacturing process of the semiconductor device which is provided with an aluminum titanium nitride layer formed so as to form an oxide dielectric layer on a conductive oxide layer. Fig. 20 is a diagram which also indicates a cross sectional structure of a scribing area of a silicon wafer according to an embodiment of the present invention.

#### Best mode for Carrying out the Invention

Hereunder, the preferred embodiments of the present invention will be described. How to form a capacitor using oxide dielectrics and how to apply the capacitor to an actual semiconductor device will be described separately. The former way is further described by the conductive material selection guideline described above.

#### 1. How to Form an Oxide Dielectric Capacitor

##### 1-1 Guideline 1 for selecting conductive materials

At first, a description will be provided for the first to third preferred embodiments of the present invention with reference to the accompanying drawings if a double-layered conductive oxide layer is selected for two conductive oxide layers provided between a semiconductor layer and a dielectric layer in an electrode of an oxide dielectric capacitor suitable for a semiconductor device.

<First Embodiment>

In the first embodiment of the present invention, the resistance of the lower electrode layer and the polarization hysteresis curve of an oxide ferroelectric capacitor were measured with respect to the lower electrode layer 11 formed so as to form a conductive oxide layer 14 with oxygen deficiency in a double-layered conductive oxide layer 12 shown in Fig. 2 directly on a polycrystalline silicon layer 20.

At first, an amorphous silicon layer doped with phosphorus of 150nm in thickness was formed on a 15mm square conductive silicon substrate 10 by chemical vapor deposition. The substrate was then annealed thereby obtaining a conductive polycrystalline silicon layer 20. Then, two types of samples were formed on this substrate. One sample was formed as follows; at first, conductive oxide layers 14 and 15 were formed through a 2mm square metal mask, then they were further shrunken down to a 100  $\mu\text{m}$  square by electron beam lithography. This sample was used for measuring the resistance of the object electrode. The other sample was formed as follows; at first, conductive oxide layers 14 and 15 were formed on the entire surface of the substrate, then an oxide dielectric layer 16 and the upper electrode layer 17 were stacked like a pyramid through a 4mm square metal mask and another metal mask of 2mm in diameter, respectively. Then, the upper electrode layer 17 was shrunken down to a 10 $\mu\text{m}$  square by ion milling using a photo mask. This sample was used for measuring the characteristics of the object capacitor.

To form the conductive oxide layers 14 and 15,  $\text{IrO}_2$ ,  $\text{RuO}_2$ ,  $\text{SrRuO}_3$ ,  $\text{SrTiO}_3$  to which La was added by 4 weight%, and  $\text{ReO}_3$  were used (in this embodiment, chemical formulas are used to clarify each compound. The description of the oxygen deficiency is omitted for convenience sake). Next, how to form each oxide layer will be described. However, the methods described here for manufacturing each compound are just examples. They may be exchanged for each other.

The electron beam deposition method was used only for forming  $\text{IrO}_2$ . At first, the  $\text{IrO}_2$  oxide powder was molded into a cylindrical shape of 12mm in diameter and 10mm in thickness using a pressure die. After this, it was annealed at 1100°C for 2 hours in an oxygen gas flow. This was used as an electron beam source. Then, a  $\text{IrO}_2$  layer with oxygen deficiency was formed under the following conditions: temperature of the substrate heater; 600°C, deposition rate; 2nm/min, and pressure: 0.1  $\mu\text{Torr}$ . After this, oxygen gas was introduced up to a pressure of 70  $\mu\text{Torr}$ . At the same time, the substrate heater was set to 580°C thereby stacking a 50nm  $\text{IrO}_2$  layer to obtain a double layered conductive oxide layer 12.

The conductive oxide layers other than  $\text{IrO}_2$  were formed by the RF-magnetron sputtering method using a sintered oxide target consisting of the above cation composition. An oxide dielectric layer of 5 to 50nm in thickness with oxygen deficiency was formed on the following film deposition conditions: temperature of the substrate heater; 600°C incident power; 1.5W/cm<sup>2</sup>, deposition rate; 3nm/min, and

discharge Ar gas pressure of 3N in purity; 3 mTorr. After this, oxygen was introduced at Ar/O<sub>2</sub>=9/1 and the substrate heater was set to 580°C, thereby forming a conductive oxide layer so as to form a double-layered conductive oxide layer 12.

The oxide dielectric layer 16 was formed using the RF-magnetron sputtering method using bismuth titanate Bi<sub>4</sub>Ti<sub>3</sub>O<sub>12</sub>), which is one of the bismuth layered ferroelectrics. The target was a sintered material represented by the above cation composition. The film deposition conditions are as follows: temperature of the substrate heater; 600°C discharge gas/oxygen gas pressure ratio; Ar/O<sub>2</sub>=9/1, total pressure; 5 mTorr, incident power; 1.5W/cm<sup>2</sup>, deposition rate; 5nm/min. and thickness; 200nm. The type and preparation method of the oxide dielectric layer just affected the substantial physical properties of the capacitor. There was recognized no influence on the double-layered conductive oxide layer. On the upper electrode layer 17 there was deposited a gold film of 100nm in thickness using the electron beam deposition method.

Fig.7(a) shows the total resistance (vertical axis) of the entire lower electrode layer as a function of the thickness(horizontal axis)of the conductive oxide layer with oxygen deficiency, formed in a non-oxidizing atmosphere. The resistance was measured between the conductive oxide layer formed in an oxidizing atmosphere and the conductive silicon substrate. In any of the conductive oxide electrodes, if the oxygen deficient layer was 5nm in thickness, the electrode



resistance was very large. Thus, it was clear that polycrystal silicon was oxidized, thereby increasing the resistance. If the oxygen deficient layer was 5 to 10nm in thickness, the resistance dropped sharply and the layer was 10nm or over in thickness, then the resistance was almost constant. From this result, it was clear that the covering ratio of the surface of the polycrystal silicon increased and that the oxidization of the polycrystal silicon was suppressed. It was because of a resistivity difference affected on the conductive oxide layer itself that the electrode resistance depended on the type of the oxide electrode.

The resistivity of a conductive oxide material itself, when measured for another single layer film, was only a few tens of  $\mu\Omega\text{cm}$  or so for  $\text{IrO}_2$ ,  $\text{RuO}_2$ , and  $\text{RuO}_3$  and as low as two or three times of that even in the oxygen deficient film. As for  $\text{SrRuO}_3$ , if oxygen deficiency was introduced, the resistivity increased just within 200  $\mu\Omega\text{cm}$  to a few  $\text{m}\Omega\text{cm}$ . For  $\text{SrTiO}_3$  to which La was added by 4 weight%, the resistivity increased within a few hundreds of  $\mu\Omega\text{cm}$  to a few  $\text{m}\Omega\text{cm}$ . These results matched with the tendency shown in Fig. 7(a) and indicated that the resistivity did not increase remarkably even when the double-layered conductive oxide electrode grew adjacent to the polycrystalline silicon.

Fig.7(b) shows a polarization hysteresis curve of an oxide ferroelectric capacitor that uses oxide electrodes when the oxygen deficient layer is 30nm in thickness. There is no difference in the hysteresis curve between the types of oxide

electrodes. As shown clearly in Fig.7(b), if a conductive oxide layer adjacent to polycrystalline silicon is formed in a non-oxidizing atmosphere, both oxidation and oxygen diffusion are suppressed. It is thus possible to prove that a voltage supplied from the substrate can be applied effectively to the oxide dielectric layer.

#### <Second Embodiment>

In the second embodiment of the present invention, the resistance of the lower electrode layer and the polarization hysteresis curve of the oxide ferroelectric capacitor were measured with respect to the structure of the lower electrode layer 11. In the lower electrode layer 11 provided in the double-layered conductive oxide layer 12 shown in Fig. 3, the conductive oxide layer 14 with oxygen deficiency is formed on a conductive nitride layer which functions as an anti-diffusion non-oxide conductive layer 30.

At first, an amorphous silicon film with a thickness of 150nm was formed on the 15mm square conductive silicon substrate 10 using the chemical vapor deposition while doping with phosphorus. Then, the amorphous silicon film was annealed thereby to form a conductive polycrystalline silicon layer 20. After this, a conductive nitride layer, which would function as an anti-diffusion non-oxide conductive layer 30, was formed all over the substrate. On this ground layer was formed two types of samples. One sample was formed as follows; conductive oxide layers 14 and 15 were formed through a 2mm square metallic mask, then the layers 14 and 15 were shrunk down to

100  $\mu\text{m}$  square by electron beam lithography. The sample was used for measuring electrode resistance. The other sample was formed as follows; conductive oxide layers 14 and 15 were formed all over the surface of the substrate, then an oxide dielectric layer 16 and an upper electrode layer 17 were stacked like a pyramid through a 4mm square metallic mask and a 2mm diameter metallic mask, respectively, and further the upper electrode layer 17 was shrunken down to a 10  $\mu\text{m}$  square by electron beam lithography. The sample was used for measuring capacitor characteristics.

In this embodiment, TiN and TaN were used as a conductive nitride layer (anti-diffusion non-oxide conductive layer 30), which will be described below in detail. The film deposition method and the obtained results were also the same with respect to Zr, Nb, V, and W nitrides. A conductive nitride layer was formed using a DC sputtering method using a metal target. The film deposition conditions were as follows: temperature of the substrate heater; 300°C, discharge gas/nitrogen gas pressure ratio; Ar/N<sub>2</sub> = 50/50, total pressure; 4 mTorr, incident power; 400W, and film thickness: 40nm. The RF-magnetron sputtering method can also be used for forming the conductive nitride layer. The method may use a nitride target instead of the metallic target. After the film deposition, an annealing treatment was applied to the sample so as to accelerate crystallization using the rapid thermal annealing method at 800°C for two minutes in an ammonia gas atmosphere.

For the conductive oxide layers 14 and 15, compounds of  $\text{IrO}_2$ ,  $\text{RuO}_2$ ,  $\text{SrRuO}_3$ ,  $\text{CaRuO}_3$  and  $\text{ReO}_3$  were used respectively. (Chemical formula were just used to clarify each compound here. The description of the amount of oxygen deficiency was omitted for the convenience sake.) Each oxide layer was formed as follows. Each deposition method described here was just an example. The deposition method could also be replaced with another.

The compound  $\text{IrO}_2$  was formed in a weak oxidizing atmosphere using the RF-magnetron sputtering method. The target was a sintered oxide one. The film deposition conditions were as follows: temperature of the substrate heater;  $600^\circ\text{C}$ , incident power;  $1.5\text{W}/\text{cm}^2$ , discharge gas; Ar gas of 3N in purity and 3 mTorr in pressure, and weak oxidizing gas;  $\text{N}_2\text{O}$  gas of  $\text{Ar}/\text{N}_2\text{O}=100/1$  in flow ratio. Under those conditions, a conductive oxide layer with oxygen deficiency was formed with a film thickness of 5 to 50nm. Then, the gas flow ratio was lowered to  $\text{Ar}/\text{N}_2\text{O}=9/1$ , as well as the total pressure was set to 5 mTorr and the temperature of the substrate heater was set to  $580^\circ\text{C}$  to form a 50nm conductive oxide layer, thereby forming a double-layered conductive oxide layer 12.

$\text{SrRuO}_3$  and  $\text{CaRuO}_3$  were formed in an Ar gas atmosphere using a RF-magnetron sputtering method that employs a sintered oxide target. The film deposition conditions were as follows: temperature of the substrate heater;  $600^\circ\text{C}$  incident power;  $1.5\text{W}/\text{cm}^2$ , and discharge gas; Ar gas of 3N in purity and 3 mTorr

in pressure. Under those conditions, a conductive oxide layer with oxygen deficiency was formed with a film thickness of 5 to 50nm. Then, oxygen was introduced at a gas flow ratio of  $\text{Ar}/\text{O}_2=9/1$ , and the total pressure was set to 5 mtorr and the temperature of the substrate heater was set to 580°C to form a 50nm conductive oxide layer, thereby forming a double-layered conductive oxide layer 12.

$\text{RuO}_2$  and  $\text{ReO}_3$  were formed in a weak oxidizing atmosphere using the reactive evaporation method. A metal block was used as the evaporation source. The film deposition conditions were as follows: temperature of the substrate heater; 600°C, deposition rate; 1nm/min, and oxygen pressure; 5  $\mu\text{Torr}$ . Under those conditions, an oxygen deficient layer was formed with a thickness of 5 to 50nm, then oxygen was introduced at a pressure up to 70  $\mu\text{Torr}$ , and the temperature of the substrate heater was lowered to 580°C thereby to stack the 50nm thick  $\text{RuO}_2$  and  $\text{ReO}_3$  layers, so that a double-layered conductive oxide layer 12 was formed.

For the oxide dielectric layer 16, lead zirconate titanate [ $\text{Pb}(\text{Zr}_{0.5}\text{Ti}_{0.5})\text{O}_3$ ] was used. The RF-magnetron sputtering method was used to form the layer 16. The target was a sintered one represented by the above cationic composition. The film deposition conditions were as follows: temperature of the substrate heater; 600°C, discharge gas/oxygen gas pressure ratio;  $\text{Ar}/\text{O}_2=9/1$ , total pressure; 5 mTorr, incident power; 1.5W/cm<sup>2</sup>, deposition rate; 5 nm/min, and film thickness; 200nm. The type and film deposition method of the oxide dielectric

layer affected only the substantial physical characteristics of the capacitor and did not affect the double-layered conductive oxide film. The upper electrode layer 17 was formed with the same conductive oxide as that of the lower electrode layer in an oxidizing atmosphere using the RF-magnetron sputtering method. The film thickness was 80nm.

TiN (Fig. 8(a)) and TaN (Fig. 8(b)) were used respectively for forming the anti-diffusion non-oxide conductive layer 30. The resistance (vertical axis) of the entire lower electrode layer was shown as a function of the thickness(horizontal axis) of the oxygen deficient layer. The resistance was measured between the conductive oxide layer formed in an oxidizing atmosphere and the conductive silicon substrate. The resistance depended on the thickness of the oxygen deficient layer in the same way as the above regardless of the type, deposition method, and deposition conditions of the nitride layer and the conductive oxide electrode. The electrode resistance was significantly high when the oxygen deficient layer was 5nm in thickness. This was because the interface was oxidized, thereby the resistance was increased when the coating ratio of the nitride layer surface was small and a conductive oxide layer was formed in the subsequent oxidizing atmosphere. The resistance was reduced sharply as the thickness was between 5nm and 10nm and almost constant at 10nm or over. This was because the coating rate of the nitride layer surface was increased, and thereby the oxidization of the phase boundary was suppressed. The reason why the

resistance was high when using  $\text{CaRuO}_3$  or an oxide electrode was an increase of the contact resistance at the electrode interface. This was confirmed using the X ray diffraction method. As for an electrode including  $\text{IrO}_2$ ,  $\text{RuO}_2$  and  $\text{ReO}_3$ , layers formed in a weak-oxidizing atmosphere, the resistance was slightly larger than that of an electrode including  $\text{SrRuO}_3$  formed in the Ar gas. In any compounds, it was clear that the resistance was kept low enough to be used for the object electrode layer. The resistivity of a conductive oxide material itself was as described in the first embodiment of the present invention when measured for the respective single layer film of  $\text{IrO}_2$ ,  $\text{RuO}_2$ ,  $\text{ReO}_3$ ,  $\text{SrRuO}_3$ , and  $\text{SrTiO}_3$  obtained by adding La by 4 weight%. The resistivity of the  $\text{CaRuO}_3$ , when the film was formed in a non-oxidizing atmosphere, increased up to a little less than several hundreds of  $\mu\Omega\text{cm}$  to  $10\text{ m}\Omega\text{cm}$ . These results coincide with the tendency shown in Fig. 8(a), indicating that the resistance did not increase so much even when the double-layered conductive oxide electrodes grew adjacent to the anti-diffusion non-oxide conductive layer 30.

Fig. 8(c) shows a polarization hysteresis curve of an oxide ferroelectric capacitor when the oxygen deficient layer is 10nm in thickness in a case where  $\text{TiN}$  is used as a nitride layer. For an electrode that includes a  $\text{CaRuO}_3$  layer, the hysteresis curve is opened to the horizontal axis more than those of other electrodes. This seems to be because of the decomposed  $\text{CaO}$  comes the distribution in the electric field which is applied to dielectrics. However, there is no

problem, since characteristics are good enough for the capacitor. As shown in Fig. 8(c) clearly, it is proved that if a conductive oxide layer is formed adjacent to a nitride layer in a non-oxidizing atmosphere, both oxidation and oxygen diffusion are suppressed, thereby a voltage can be applied to the oxide dielectric layer effectively from the substrate. The same hysteresis curve as that shown in Fig. 8(c) was also obtained for the TaN layer.

<Third Embodiment>

In the third embodiment of the present invention. the polarization hysteresis curve for an oxide ferroelectric capacitor was measured with respect to the structure of the lower electrode layer 11, in which the conductive oxide layer 14 with oxygen deficiency is formed on an anti-diffusion non-oxide conductive layer 30 via metallic layer 40. The layer 14 is provided in the double-layered conductive oxide layer 12 shown in Fig. 4.

The shapes and film deposition methods of the substrate 10, the polycrystalline silicon layer 20, a TiN layer or the anti-diffusion non-oxide conductive layer 30, as well as the oxide dielectric layer 16 and the upper electrode layer 17 are the same as those in the first and second embodiments described above. It is not essential to select the materials of the oxide dielectric layer and the upper electrode layer, however, mentioned in the embodiments of the present invention.

The TiN layer was formed with a thickness of 40nm in



accordance with the method of the second embodiment. The TiN layer was used as an anti-diffusion non-oxide conductive layer 30. The same results were also obtained for other nitrides listed in the above second embodiment.

5 In this embodiment, platinum was used for the metallic layer 40. The same effect was also found when iridium and ruthenium, which are the same nobles metals as platinum, were used. The DC sputtering method was used for forming the metallic layer on the following conditions: Incident  
10 power; 400W, discharge gas; Ar, gas pressure; 20 mTorr, and temperature of the substrate heater: 500°C. The metallic layer 40 was thus formed with a thickness of 20nm on the whole area of anti-diffusion non-oxide conductive layer 30.

15 IrO<sub>2</sub>, RuO<sub>2</sub>, SrRuO<sub>3</sub>, and SrTiO<sub>3</sub>, which La was added by 4 weight% were used for forming the conductive oxide layer using a RF-magnetron sputtering method in a weak oxidizing atmosphere. The targets were made of a sintered oxide. The film deposition conditions were as follows: temperature of the substrate heater; 600°C incident power; 1.5W/cm<sup>2</sup>, discharge  
20 gas; Ar gas of 3N in purity and 3 mTorr in pressure. and weak oxidizing gas: N<sub>2</sub>O gas of Ar/N<sub>2</sub>O=100/1 in flow ratio. Under these conditions, the conductive oxide layer 14 with oxygen deficient layer of 10nm in thickness was formed. Then, the gas flow ratio was lowered to Ar/N<sub>2</sub>O=9/1, as well as the total  
25 pressure was set to 5 mTorr and the substrate heater was set to 580°C to form a 50nm thick conductive oxide layer 15, thereby forming a double-layered conductive oxide layer 12.

Fig. 9 shows a polarization hysteresis curve of an oxide ferroelectric capacitor with respect to each conductor oxide. Regardless of the oxygen deficient layer type, the hysteresis curve was an open one with high symmetry. Even when the metallic layer was as thin as 20nm and a conductor oxide layer adjacent to this metallic layer was formed in a weak oxidizing atmosphere, the oxygen deficient layer included in the conductive oxide layer was found to be effective for suppressing oxidation and oxygen diffusion, thereby a voltage could be applied effectively to the oxide dielectric layer from the substrate.

As described above in each of the embodiments of the present invention, a conductive oxide layer with oxygen deficiency was formed in a non-oxidizing atmosphere, which is one of the characteristics of the present invention, thereby forming a double-layered conductive oxide layer. Consequently, the lower electrode layer and the oxide dielectric layer could be formed without oxidizing the polycrystalline silicon (the first embodiment of the present invention) adjacent to the double-layered conductive oxide layer, the anti-diffusion non-oxide conductive layer consisting of nitrides, etc. adjacent to the double-layered conductive oxide layer, as well as the anti-diffusion non-oxide conductive layer (the second embodiment of the present invention) adjacent to the double-layered conductive oxide layer through a metallic layer. Consequently, it was possible to reduce the interfacial resistance and contact resistance of each electrode, thereby

forming an oxide dielectric capacitor suitable for high integration.

## 1-2 Guideline 2 for Selecting Conductive Materials

Hereunder, a description will be made to indicate how to select an aluminum titanium nitride layer at the side of the semiconductor and an anti-oxidization metallic layer at the side of the dielectrics of the two conductive material layers provided between a semiconductor layer and a dielectric layer in the electrode of an oxide dielectric capacitor suitable for a semiconductor device. The accompanying drawings will be referenced for describing the fourth and fifth embodiments of the present invention.

<Fourth Embodiment>

In the fourth embodiment of the present invention, the allowable contents of both aluminum and nitrogen were checked in an aluminum titanium layer with respect to the phase uniformity, low resistivity, and resistance to oxidation. The phase uniformity and the resistance to oxidation were checked by the X ray diffraction method and the resistivity was measured using the DC four-point probe method.

At first, an aluminum titanium nitride  $[\text{Ti}_{1-x}\text{Al}_x]_{1-y}\text{N}_y$  film was formed on a conductive silicon substrate using the DC sputtering method. A natural oxidized film was already removed from the substrate before this deposition. The target was a composite one obtained by spreading aluminum and titanium metallic plates in a mosaic fashion all over an aluminum metal plate. The aluminum content  $x$  was adjusted according to the

area ratio of both metallic plates. The nitrogen content y was adjusted by changing the argon discharge gas/nitrogen gas flow ratio within the range of 95/5 to 5/95. The substrate heater was set to 550°C. Other film deposition conditions were as follows: Incident power; 400W, total gas pressure; 5 to 20 mTorr, growth rate; 5 to 10 nm/min, and film thickness; 50nm. The aluminum content x was analyzed and determined using the ICPS method (Inductively-Coupled Plasma Spectroscopy) and the nitrogen content y was analyzed and determined using the RBS (Rutherford Back Scattering) method that uses He<sup>+</sup> ions.

Fig. 10(a) shows both reaction products and the resistivity of a sample whose nitrogen content y is 0.5 as a function of the aluminum content x. As a result of X ray diffraction, only a diffraction line assignable to TiN was observed when x was 0.6 or below. If x exceeded 0.6, however, a mixed phase with a phase assignable to AlN was observed. As the x value increased, the TiN phase disappeared and the AlN phase increased. The resistivity increased a little as the x value increased. The resistivity increased sharply around 0.5.

Fig. 10(b) shows both reaction products and resistivity of a sample whose aluminum content x is 0.4 as a function of the nitrogen content y. As a result of X ray diffraction, diffraction lines other than TiN were observed if the y value was smaller than 0.2 or exceeded 0.6. The resistivity was checked only for the nitrogen content whose y value was 0.2 to 0.6 (included). For this nitrogen content, a single phase was observed in the X ray diffraction pattern. The resistivity

increased as the y value increased. And, the resistivity increased sharply around 0.6 of the y value. Usually, an effect of the impurity phase is observed in the resistivity more than in X ray diffraction. Thus, the threshold values of both x and y to be determined by a resistivity seems to be narrowed.

Next, a platinum layer with a thickness of 30nm was formed by the DC sputtering method on the aluminum titanium layer formed above. The film deposition conditions were as follows: Incident power; 400W, discharge gas; Argon gas, gas pressure; 20 mTorr, and deposition temperature; 500°C. On the platinum layer was stacked an oxide dielectric layer  $[\text{Pb}(\text{Zr}_{0.5}\text{Ti}_{0.5})\text{O}_3]$  with a thickness of 100nm, using RF-magnetron sputtering. The film deposition on conditions were as follows: temperature of the substrate heater; 300°C, incident power; 1.5W/cm<sup>2</sup>, deposition rate; 3 nm/min, discharge Ar gas/oxygen gas flow ratio; 90/10, and pressure; 5 mTorr. After the 100nm thick oxide dielectric layer was formed, rapid thermal annealing was applied to the layer at 650°C for 2 minutes in an oxygen flow, thereby to accelerate the crystallization of the layer.

Finally, the oxide dielectric layer, after it was formed once, was removed completely in a dry etching process, thereby exposing the platinum layer again. An X ray diffraction measurement was made for this sample to check if the aluminum titanium nitride  $[(\text{Ti}_{1-x}\text{Al}_x)_{1-y}\text{N}_y]$  layer was oxidized and changed in quality by the formed oxide dielectric layer. Fig. 10(a)

also shows this result. As shown in Fig. 10(a), it was confirmed that the oxide layer was oxidized, thereby  $\text{TiO}_2$  was formed when the aluminum content x was smaller than 0.2. And, as shown in Fig. 10(b),  $\text{TiO}_2$  was also observed when the nitrogen content y was smaller than 0.4.

The above threshold values remained the same even when both aluminum and nitrogen contents x and y were fixed at another value respectively.

The above threshold values also remained the same substantially even when platinum was replaced with any of iridium, ruthenium, and rhenium for forming the metallic layer. And, the aluminum titanium nitride layer for preventing oxygen diffusion and oxidation was also effective for other oxide dielectrics, for example, lead zirconate titanate having a different titanium/zirconium ratio, lead barium zirconate titanate, barium strontium titanate, and bismuth ferroelectrics.

#### <Fifth Embodiment>

In the fifth embodiment of the present invention, the polarization hysteresis curve of an oxide dielectric capacitor including an aluminum titanium nitride layer for preventing oxygen diffusion and oxidation was measured (Fig. 11).

For the sample (a), an oxide dielectric layer was stacked directly on the platinum layer of 30nm in thickness/aluminum titanium nitride layer of 50nm in thickness/conductive silicon substrate described in the fourth embodiment of the present invention. For the sample (b), an oxide dielectric layer was

stacked on the above layer through a conductive oxide layer.

A  $\text{RuO}_2$  layer of 50nm in thickness was formed as the conductive oxide layer using the RF-magnetron sputtering method. The target was an Ru metal one. The film deposition conditions were as follows: temperature of the substrate heater; 500°C, incident power; 1.5W/cm<sup>2</sup>, deposition rate; 3 nm/min, discharge Ar gas/oxygen gas flow ratio; 50/50, and pressure; 7mTorr.

Lead zirconate titanate [ $\text{Pb}(\text{Zr}_{0.5}\text{Ti}_{0.5})\text{O}_3$ ] layer of 100nm in thickness was formed as the oxide dielectric layer using the sol-gel method. Sol was a solution obtained by making lead acetate, titanium isopropoxide and zirconium isopropoxide react with each other in methoxy ethanol. This solution was coated on the platinum layer [sample (a)] or on the conductive oxide layer [sample (b)], then rapid thermal annealing was applied to each sample at 650°C for two minutes in an oxidizing atmosphere, thereby crystallizing the sample.

A 2mm diameter platinum layer was formed as the upper electrode layer through a metallic mask using the DC sputtering method.

Fig. 11 shows a polarization hysteresis curve measured when a voltage was applied between the upper electrode layer and the conductive silicon substrate. For both samples(a) and (b), good hysteresis curves were obtained. Even when the platinum layer put therebetween was as thin as 30nm, the aluminum titanium nitride layer functioned effectively to prevent oxygen diffusion and oxidation. It was thus confirmed

that the object capacitor operation was satisfactory with a voltage supplied from the substrate.

To select certain materials of a conductive oxide layer and an oxide dielectric layer is not essential in the embodiments of the present invention. For example, any of the conductive oxides of  $\text{IrO}_2$ ,  $\text{SrRuO}_3$ , and  $\text{ReO}_3$  can be used to obtain the same effect. In addition, any of lead zirconate titanate  $[\text{Pb}(\text{Zr}_x\text{Ti}_{1-x})\text{O}_3]$  with  $x$  other 0.5, lead strontium barium titanate  $[(\text{Ba}_x\text{Sr}_{1-x})\text{TiO}_3 (x=0 \text{ to } 1)]$ , barium zirconate titanate, and bismuth layered ferroelectrics can be used to form the object capacitor in the same way.

As described in each of the embodiments of the present invention, if an aluminum titanium nitride layer for preventing oxygen diffusion and oxidation, which is one of the characteristics of the present invention, was formed, then the lower electrode layer and the oxide dielectric layer could be formed without oxidizing the nitride layer even when adjacent metallic layers including the platinum one were thinned down to 30nm. Consequently, the interfacial resistance and the contact resistance of each electrode, as well as the capacitor aspect ratio could be reduced, thereby forming an oxide dielectric capacitor suitable for high integration.

## 2. How to Form a Semiconductor Device Provided with a Dielectric Capacitor

Next, description will be made for how an oxide dielectric capacitor of the present invention is used in a



semiconductor device. A MOS transistor formed on a silicon substrate will be picked up as an example for the description with reference to the accompanying drawings with respect to the sixth to tenth embodiments of the present invention to be described below. The sixth to eighth and ninth to tenth embodiments are based on the guideline 1 and 2 for selecting conductive materials respectively as described above.

<Sixth Embodiment>

In this sixth embodiment of the present invention, description will be made at first for the pre-process up to the forming of an oxide dielectric capacitor with respect to the manufacturing method of a semiconductor device.

At first, description will be made for how to form a MOS transistor on a silicon substrate, then how to planarize the surface of the substrate once and finally for how to form a polycrystalline silicon plug used to connect the capacitor electrode electrically to the MOS transistor. The series of manufacturing processes will be described sequentially with reference to Figs. 12 to 15.

As shown in Fig. 12, a switching transistor is formed in an existing MOSFET integrating process. Reference numeral 121 denotes a p-type semiconductor substrate, 122 denotes an isolating insulator between devices, 123 denotes a gate oxide film, 124 denotes a word line used as a gate electrode, and 125 and 126 denote n-type impurity diffusion layers in which phosphorus is doped respectively. Reference numeral 127 denotes a passivation layer consisting of  $\text{SiO}_2$ . Next, the

surface is covered completely with a 50nm thick  $\text{SiO}_2$  layer 128 by the chemical vapor deposition. After this, the surface is covered once with a 600nm thick  $\text{Si}_3\text{N}_4$  layer 129, then this  $\text{Si}_3\text{N}_4$  layer 129 is etched as deep as the deposited film thickness, thereby filling the insulator between word lines. The structure is thus formed as shown in Fig. 12. The  $\text{SiO}_2$  layer 128 is an under layer for producing the bit lines in a subsequent process and is used to prevent exposure of the surface of the substrate, as well as damage to the isolating insulator 122 between elements.

Fig. 13 shows the next process. The  $\text{Si}_3\text{N}_4$  portion where a bit line to be formed later will come in contact with the n-type impurity diffusion layer 125 on the surface of the substrate, as well as the  $\text{Si}_3\text{N}_4$  portion where a capacitor electrode to be formed later will come in contact with the n-type impurity diffusion layer 126 on the surface of the substrate are processed respectively so as to be perforated with holes using a photo-lithography method and a dry etching method. After this, amorphous silicon including an n-type impurity is deposited with a thickness of 600nm all over the portion including the holes, and then is annealed so as to be crystallized. The polycrystalline silicon is then etched as deep as the film thickness, so as to be structured as shown in Fig. 13. Consequently, the holes are filled with polycrystalline silicon 131 and 132.

Fig. 14 shows the next process for forming a bit line. At first, the entire surface is covered with the  $\text{SiO}_2$  insulator

141 using the chemical vapor deposition. Then, the  $\text{SiO}_2$  insulator positioned above the polycrystalline silicon 131 is perforated with holes using both photo-lithography method and dry etching method so that the bit line to be formed later are connected to the n-type impurity diffusion layer 125 electrically. After this, metallic silicide to become a bit line later, as well as a polycrystalline silicon layer (142) are formed all over these holes. And, on the layer 142 is deposited an  $\text{SiO}_2$  layer 143 with a thickness of 200 nm. The  $\text{SiO}_2$  layer 143, the metallic silicide, and the polycrystalline silicon layer 142 are then patterned using both photo-lithography and dry-etching methods, thereby forming a bit line 142 and an  $\text{SiO}_2$  layer 143. Then, to insulate the side wall of the bit line 142,  $\text{Si}_3\text{N}_4$  deposited with a thickness of 150nm using the chemical vapor deposition, then etched using the dry-etching method, thereby forming an  $\text{Si}_3\text{N}_4$  side wall spacer 144. Finally, the  $\text{SiO}_2$  insulator 141 positioned above the polycrystalline silicon 132 is treated using both photo-lithography and dry-etching methods, thereby making holes. These holes are used to connect a capacitor electrode to be formed later to the n-type impurity diffusion layer 126 electrically.

Fig. 15 shows the process for planarizing the surface of the substrate and forming a conductive polycrystalline silicon plug before the object capacitor is formed. At first, an insulator 151 is deposited on the substrate with a thickness sufficient to planarize the surface of the

substrate. In this embodiment of the present invention, a 500nm thick boron phosphorus silicate glass (BPSG) is used, but another silicon oxide film may be used instead of the BPSG. The glass is planarized by chemical mechanical polishing. The surface of the substrate can also be covered by  $\text{SiO}_2$  using the chemical vapor deposition, then etched back to planarize the surface. Next, the photo-lithography and the dry etching method are applied to the insulator 151 positioned above the n-type impurity diffusion layer 126, thereby making contact holes. After this, phosphorus-doped amorphous silicon is deposited all over the surface including those holes with a thickness of 200nm using the chemical vapor deposition, and then it is annealed to crystallize the surface. The surface is then etched back using the dry etching method, thereby forming each polycrystalline silicon plug 152 filled with polycrystalline silicon.

This completes the pre-process for forming the oxide dielectric capacitor.

Next, description will be made for respective processes for forming an oxide dielectric capacitor including a double-layered conductive oxide later on the substrate for which a MOS transistor and a polycrystalline silicon plug are already formed. In this embodiment, the lower electrode takes a structure in which a conductive oxide layer with oxygen deficiency is formed directly on the polycrystalline silicon shown in Fig. 2.

At first, as shown in Fig. 16, a 10nm thick conductive

oxide layer 161 ( $\text{RuO}_2$ ) with oxygen deficiency is formed in an Ar atmosphere using the RF-magnetron sputtering method as described in detail in the first embodiment of the present invention. Then, oxygen is introduced at a gas flow ratio up to  $\text{Ar}/\text{O}_2=9/1$ , and the total pressure is increased as well, thereby stacking a 50nm thick conductive oxide layer 162 so as to form a double-layered conductive oxide layer (161 and 162). After this, the layer(161 and 612) was covered with a 50nm thick W film using the DC sputtering method. Then, a photoresist masking pattern was transferred onto the surface of the layer (161 and 162) using the dry etching method. This transferred pattern was used as a mask to pattern the double-layered conductive oxide layer (161 and 162) using the sputtering etching method. Then, the transferred mask was removed by etching and an oxide dielectric layer 163 was formed. In the embodiments of the present invention, lead zirconate titanate  $[\text{Pb}(\text{Zr}_{0.5}\text{Ti}_{0.5})\text{O}_3]$  was used as an oxide dielectric. The deposition method was as described in detail in the second and third embodiments of the present invention. The film thickness was 100nm. Finally, a platinum cell plate electrode 164 was formed to complete the object memory cell capacitor.

The polarization hysteresis characteristics of the oxide ferroelectric capacitor (sample) were measured by changing the capacitor area from 0.2 to 25  $\mu\text{m}^2$ . As a result, a satisfactory hysteresis curve was obtained, enabling a voltage to be supplied to the oxide dielectric layer from the

polycrystalline silicon plug 152 in any cases.

In the embodiments of the present invention, it is not essential to select a particular material for the oxide dielectric layer. Any of lead zirconate titanate  $[\text{Pb}(\text{Zr}_y\text{Ti}_{1-y})\text{O}_3]$  with  $y$  other than 0.5, strontium barium titanate  $[\text{Ba}_x\text{Sr}_{1-x}\text{TiO}_3 (X=0 \text{ to } 1)]$ , lead barium zirconate titanate, and bismuth layered ferroelectrics can be used to form memory cells in the same way. In addition, the same effect could be obtained for the conductive oxide layer using any of the compounds described in the first embodiment of the present invention.

<Seventh Embodiment>

In this seventh embodiment of the present invention, description will be made of a process for forming an oxide dielectric capacitor on a substrate after finishing the processes from forming a MOS transistor up to forming a polycrystalline silicon plug as described in detail in the sixth embodiment of the present invention. The capacitor includes a double-layered conductive oxide layer formed on an anti-diffusion non-oxide conductive layer as shown in Fig. 3.

At first, as shown in Fig. 17, an anti-diffusion oxide conductive layer 171 is formed. In this embodiment,  $\text{TiN}$  is used for the anti-diffusion non-oxide conductive layer and such an example will be described in detail. However, note that the same effect was also obtained for the semiconductor device of the present invention when any of, the nitrides of

Ta, Zr, Nb, V, and W were used. The nitride layer, as described in detail in the second embodiment of the present invention, was formed using the DC sputtering method that employed a metallic target. The film thickness was 40nm. After the film deposition, the sample was annealed at 800°C for two minutes in an ammonia gas atmosphere using the rapid thermal annealing method, thereby accelerating the crystallization of the film.

Next, an  $\text{SrRuO}_3$  layer was formed in a weak oxidizing atmosphere using the RF-magnetron sputtering method. The layer was used as a double-layered conductive oxide layer. The same effect can be obtained even with the film deposition in an Ar gas atmosphere. Then, a conductive oxide layer 161 ( $\text{SrRuO}_3$ ) with a 10nm thick oxygen deficient layer was formed at a gas flow ratio of  $\text{Ar}/\text{O}_2=100/1$ , and then the gas flow ratio was lowered to  $\text{Ar}/\text{O}_2=9/1$  thereby stacking a 50nm conductive oxide layer 162 so as to form the double-layered conductive oxide layer (161 and 162). The film deposition conditions including the temperature were the same as those in the second embodiment of the present invention described above.

Next, the above layers were covered with a 50nm W film and a photo-resist masking pattern was transferred to the W film using the dry etching method. This transferred pattern was used as a mask for patterning the double-layered conductive oxide layer (161 and 162), as well as the anti-diffusion non-oxidizing conductive layer 171 through sputter-etching. The transferred mask was then removed and an oxide

dielectric layer 163 was formed. In the embodiments of the present invention, lead zirconate titanate  $[Pb(Zr_{0.5}Ti_{0.5})O_3]$  was used as an oxide dielectric. The film deposition method was the same as described in the second and third embodiments of the present invention in detail. The film thickness was 100nm. Finally, a platinum electrode 164 was formed to complete the object capacitor of a memory cell.

The sample was then measured with respect to the polarization hysteresis characteristics of this oxide ferroelectric capacitor by changing the capacitor area from 0.2 to 25  $\mu m^2$ . As a result, it was found in all cases that a voltage could be supplied from the polycrystal silicon plug 152 to the oxide dielectric layer so as to obtain a satisfactory hysteresis curve.

In the embodiments of the present invention, it is not essential to select a particular material for the oxide dielectric layer. Any of lead zirconate titanate  $[Pb(Zr_xTi_{1-x})O_3]$  with x other than 0.5, strontium barium titanate  $[(Ba_xSr_{1-x})TiO_3]$  (X=0 to 1)], lead barium zirconate titanate, and bismuth layered ferroelectrics can be used to form memory cells. The same effect could also be obtained using any of the compounds,  $IrO_2$ ,  $RuO_2$ ,  $CaRuO_3$ ,  $SrTiO_3$  to which La is added, and  $ReO_3$  for the conductive oxide layer as described in the first to this embodiments of the present invention.

#### <Eighth Embodiment>

In this eighth embodiment of the present invention, description will be made of a process for forming an oxide



dielectric capacitor on a substrate after finishing the processes from forming of a MOS transistor up to forming of a polycrystalline silicon plug as described in detail in the sixth embodiment of the present invention. The capacitor includes a double-layered conductive oxide layer formed on an anti diffusion non-oxide conductive layer through a metallic layer as shown in Fig. 4.

At first, as shown in Fig. 18, an anti-diffusion oxide conductive layer 171 is formed. In this embodiment, TiN is used for the anti-diffusion non-oxide conductive layer and such an example will be described below. However, note that the same effect was also obtained for the semiconductor device of the present invention when any of the nitrides of Ta, Zr, Nb, V, and W was used. The TiN layer was formed as described in detail in the seventh embodiment of the present invention. On this layer a 20nm thick metallic layer 181 was formed using the DC sputtering method. Although platinum was used in this embodiment, it was confirmed that the same effect was also obtained with the use of iridium and ruthenium. The film deposition conditions for the metallic layer were the same as those in the third embodiment of the present invention.

Next, an  $\text{IrO}_2$  layer was formed in a weak oxidizing atmosphere using the RF-magnetron sputtering method. The layer was used as a double-layered conductive oxide layer. Of course, the same effect was obtained even with the film deposition in an Ar gas atmosphere. Then, a 10nm conductive oxide layer 161 ( $\text{IrO}_2$ ) with oxygen deficiency was formed at a

gas flow ratio of  $\text{Ar}/\text{O}_2=100/1$ , then the gas flow ratio was lowered to  $\text{Ar}/\text{O}_2=9/1$  so as to stack a 50nm conductive oxide layer 162 ( $\text{IrO}_2$ ), thereby forming a double-layered conductive oxide layer (161 and 162). The film deposition conditions including the temperature were the same as those in the third embodiment of the present invention described above.

Next, the above layer was covered with a 50nm W film and a photo-resist masking pattern was transferred to the W film using the dry etching method. This transferred pattern mask was used for patterning the double-layered conductive oxide layers 161 and 162 and metallic layer 181, as well as for the anti-diffusion non-oxidizing conductive layer 171 through sputter-etching. The transferred mask was then removed and an oxide dielectric layer 163 was formed. In the embodiments of the present invention, lead zirconate titanate  $[\text{Pb}(\text{Zr}_{0.5}\text{Ti}_{0.5})\text{O}_3]$  as used as an oxide dielectric. The film deposition method was the same as those described in the second and third embodiments of the present invention in detail. The film thickness was 100nm. Finally, a platinum cell plate electrode 164 was formed to complete the object capacitor of a memory cell.

The sample was then measured with respect to the polarization hysteresis characteristics of this oxide ferroelectric capacitor by changing the capacitor area from 0.2 to  $25 \mu\text{m}^2$ . As a result, it was found in all cases that a voltage could be supplied from the polycrystal silicon plug 152 to the oxide dielectric layer so as to obtain a

satisfactory hysteresis curve.

In the embodiments of the present invention, it is not essential to select a particular material for the oxide dielectric layer. Any of lead zirconate titanate  $[\text{Pb}(\text{Zr}_x\text{Ti}_{1-x})\text{O}_3]$  with X other than 0.5, strontium barium titanate  $[(\text{Ba}_x\text{Sr}_{1-x})\text{TiO}_3]$  (X=0 to 1), lead barium zirconate titanate, and bismuth layered ferroelectrics can be used to form memory cells in the same way. The same effect could also be obtained using any of the compounds,  $\text{RuO}_2$ ,  $\text{SrRuO}_3$ ,  $\text{CaRuO}_3$ ,  $\text{SrTiO}_3$  to which La is added, and  $\text{ReO}_3$  as described in the first to third embodiments of the present invention for the conductive oxide layer.

<Ninth Embodiment>

In this ninth embodiment of the present invention, description will be made of a process for forming an oxide dielectric capacitor on a substrate after finishing the processes from forming of a MOS transistor up to forming of a polycrystalline silicon plug as described in detail in the sixth embodiment of the present invention. The capacitor includes an aluminum titanium nitride layer for preventing oxygen diffusion and oxidation. In this embodiment, the lower electrode layer takes a structure in which a metallic layer and an oxide dielectric layer are stacked sequentially on the aluminum titanium nitride shown in Fig. 5.

At first, as shown in Fig. 19, an aluminum titanium nitride  $[\text{Ti}_{0.7}\text{Al}_{0.3}]_{0.5}\text{N}_{0.5}$  layer 191 was formed using the RF-magnetron sputtering method. The target was a composite one obtained by depositing a proper amount of aluminum nitride

plate on a titanium nitride plate. The film deposition conditions were as follows: temperature of the substrate heater; 550°C, incident power; 400W, total gas pressure; 8 mTorr, argon discharge gas/nitrogen gas flow ratio; 90/10, deposition rate; 10 nm/min, and film thickness; 50nm. The same effect to be described below was also obtained using another aluminum or nitrogen content as indicated in Fig. 5.

On this layer a 30nm thick metallic layer 181 was formed using the DC sputtering method. Although platinum was used in this embodiment, it was confirmed that the same effect was also obtained with the use of iridium and ruthenium. The film deposition conditions for the metallic layer were the same as those in the fourth embodiment of the present invention.

Next, the layer formed above was covered with a 50nm W film and a photo-resist masking pattern was transferred to the W film using the dry etching method. Using this transferred pattern as a mask, the aluminum titanium nitride layer 191 and the metallic layer 182 were patterned through sputter-etching. The transferred mask was then removed and an oxide dielectric layer 163 was formed. In the embodiments of the present invention, lead zirconate titanate [ $\text{Pb}(\text{Zr}_{0.5}\text{Ti}_{0.5})\text{O}_3$ ] was used as an oxide dielectric. The film deposition method was the sol-gel method as described in the fifth embodiment of the present invention in detail. The film thickness was 100nm. Finally, a platinum electrode 164 was formed and patterned to complete the object capacitor of a memory cell.

The sample was then measured with respect to the polarization hysteresis characteristics of this oxide ferroelectric capacitor by changing the capacitor area from 0.2 to 25  $\mu\text{m}^2$ . As a result, it was found in all cases that a voltage could be supplied from the polycrystal silicon plug 152 so as to obtain a satisfactory hysteresis curve.

In the embodiments of the present invention, it is not essential to select a particular material as the oxide dielectric layer. Any of lead zirconate titanate  $[\text{Pb}(\text{Zr}_x\text{Ti}_{1-x})\text{O}_3]$  with x other than 0.5, strontium barium titanate  $[(\text{Ba}_x\text{Sr}_{1-x})\text{TiO}_3]$  (X=0 to 1) lead barium zirconate titanate, and bismuth layered ferroelectrics can be used to form memory cells in the same way.

#### <Tenth Embodiment>

In this tenth embodiment of the present invention, description will be made of a process for forming an oxide dielectric capacitor on a substrate after finishing the processes from forming of a MOS transistor up to forming of a polycrystalline silicon plug as described in detail in the sixth embodiment of the present invention. The capacitor includes an aluminum titanium nitride layer for preventing oxygen diffusion and oxidation. In this embodiment, the lower electrode layer takes a structure in which a metallic layer, a conductive oxide layer, and an oxide dielectric layer were stacked sequentially on the aluminum titanium nitride shown in Fig. 5.

At first, as shown in Fig. 20, an aluminum titanium

nitride[(Ti<sub>0.5</sub>Al<sub>0.5</sub>)<sub>0.5</sub>N<sub>0.5</sub>] layer 191 and a metallic layer 181 were formed using the same method as that in the ninth embodiment. The same effect to be described, below was also obtained using another aluminum or nitrogen content, as well as using iridium, ruthenium, and rhenium.

A 50nm thick IrO<sub>2</sub> layer formed using the RF-magnetron sputtering method was used as the conductive oxide layer 201. The target was an Ir metal one. The film deposition conditions were as follows: temperature of the substrate heater; 500°C, incident power; 1.5W/cm<sup>2</sup>, deposition rate; 3 nm/min, discharge Ar gas/oxygen gas flow ratio; 50/50, and pressure: 7mTorr.

Next, the layer formed above was covered with a 50nm W film and a photo-resist masking pattern was transferred to the W film using the dry etching method. Using this transferred pattern as a mask, the aluminum titanium nitride layer 191, the metallic layer 181, as well as a conductive oxide layer 201 were patterned through sputter-etching.

The transferred mask was then removed and an oxide dielectric layer 163 was formed. In the embodiments of the present invention, bismuth layered ferroelectrics, Bi<sub>4</sub>Ti<sub>3</sub>O<sub>12</sub>, was used as the oxide dielectric. In an oxidizing atmosphere at 50 μTorr in pressure, the titanium and bismuth were evaporated using an electron gun and an effusion cell respectively, thereby forming a 100nm thick amorphous oxide layer at room temperature. After this, a rapid thermal annealing treatment was applied to the sample at 700°C for

2min in an oxygen atmosphere so as to crystallize the surface. Finally, a platinum cell plate electrode 164 was formed and patterned to complete the object capacitor of a memory cell.

5       The sample was then measured with respect to the polarization hysteresis characteristics of this oxide ferroelectric capacitor by changing the capacitor area from 0.2 to 25  $\mu\text{m}^2$ . As a result, it was found in all cases that a voltage could be supplied from the polycrystal silicon plug 10 152 to the oxide dielectric layer so as to obtain a satisfactory hysteresis curve.

Whether to select a conductive oxide layer or an oxide dielectric layer is not essential in the embodiments of the present invention. In addition, any of lead zirconate titanate 15  $[\text{Pb}(\text{Zr}_x\text{Ti}_{1-x})\text{O}_3 (x=0 \text{ to } 1)]$ , strontium barium titanate  $[(\text{Ba}_x\text{Sr}_{1-x})\text{TiO}_3 (x=0 \text{ to } 1)]$ , lead barium zirconate titanate, bismuth layered ferroelectrics, and  $\text{SrBi}_2\text{Ta}_2\text{O}_9$ , can be used to form the object capacitor in the same way. Any of the conductive oxides of  $\text{RuO}_2$ ,  $\text{SrRuO}_3$ ,  $\text{ReO}_3$ , can also be used to 20 obtain the same effect.

As described in each of the embodiments of the present invention, a MOS transistor formed on a silicon substrate is applied to a semiconductor device provided in an oxide dielectric capacitor of the present invention. As for the 25 guideline 1 for selecting conductive materials, a conductive oxide layer with oxygen deficiency was formed in a non-oxidizing atmosphere, thereby forming a double-layered

conductive oxide layer. Consequently, the object memory cell was formed without oxidizing the polycrystalline silicon (the sixth embodiment of the present invention) adjacent to the double-layered conductive oxide layer, the anti-diffusion non-oxide conductive layer consisting of a nitride, etc. (the seventh embodiment of the present invention), and the anti-diffusion non-oxide conductive layer (the eighth embodiment of the present invention) through a metallic layer. In accordance with the guideline 2 for selecting conductive materials, an aluminum titanium nitride layer for preventing oxygen diffusion and oxidation was formed, thereby stacking an oxide dielectric layer (the ninth embodiment of the present invention) and a conductive oxide layer (the tenth embodiment of the present invention) without oxidizing the nitride layer even when the metallic layer consisting of platinum, etc. and adjacent to the aluminum titanium nitride layer for preventing oxygen diffusion and oxidation was thinned down to 30nm. The object memory cell could be formed in such a way. According to the structures and film deposition methods described above. it became possible to reduce both interfacial resistance and contact resistance of the object electrode, as well as to reduce the capacitor aspect ratio. It was thus possible for the present invention to obtain a semiconductor device provided with fine-structured memory cells suitable for high integration.

In the above embodiments of the present invention, the semiconductor of the present invention was mainly applied





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## SPECIFICATION

## Title of the Invention

## SEMICONDUCTOR DEVICE AND ITS MANUFACTURING METHOD

## Technical Field

The present invention relates to a semiconductor device, suitable for <sup>which as</sup> LSIs, as well as a method <sup>Device</sup> [for] manufacturing such a semiconductor. The semiconductor device uses oxide dielectrics, especially oxide ferroelectrics <sup>in the formation of a</sup> [as its] capacitor.

## Background [Art] of the Invention

Semiconductor devices consisting of LSIs such as dynamic random access memories ( DRAMS), etc. have been confronted with problems that the capacitor area must be reduced to cope with high integration of the [object] LSI [as]. <sup>In addition,</sup> [well as] such a semiconductor device must be prevented from <sup>having a</sup> complicated structure caused by the reduction of [such] the capacitor <sup>capacity</sup> area. In order to solve <sup>these</sup> [those] problems, therefore, <sup>consideration</sup> [it] has been <sup>given</sup> [examined] to use <sup>the</sup> oxide dielectrics and oxide ferroelectrics as the insulator of the capacitor, instead of [the] silicon oxide and [the] silicon nitride <sup>which have</sup> [having] been used so far. The relative dielectric constants of both oxide

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dielectrics and oxide ferroelectrics are as large as several hundreds to several thousands. (The oxide dielectrics mentioned here do not include silicon oxides, [etc. <sup>but concern</sup> It means] <sup>Λ</sup> so-called dielectrics whose relative dielectric constants are several hundreds.) The ferroelectrics <sup>have</sup> [has] spontaneous polarization and <sup>or</sup> [its] polarity, <sup>that</sup> can be reversed using an external electric field. The reversed polarity can also be held. It has thus been <sup>proposed</sup> [tried] to use such [the] ferroelectrics for non-volatile memories. A conventional memory composed of such ferroelectrics is disclosed in the official gazette of Unexamined Published Japanese Patent Application No. Sho-63-201998 (since oxide ferroelectrics can be regarded <sup>as</sup> [to be] dielectrics at temperatures above the Curie temperature, hereunder, <sup>the term</sup> [a word of] <sup>Λ</sup> dielectrics will be used to describe the ferroelectrics representatively).

Generally, lead zirconate titanate, strontium barium titanate, and the like are used as oxide dielectrics for memories. However, it has been difficult to use oxide dielectric capacitors for semiconductor devices used as conventional memories, etc., since high temperatures above 500 °C are needed to crystallize the oxide dielectrics in an oxidizing atmosphere.

For example, it might be considered to adopt a structure (conventional structure 1; oxide dielectrics/platinum/silicon) <sup>such</sup> [so] that platinum can be used

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a <sup>which is</sup> lower electrode, resistant against both oxidation and thermal budget, provided under an oxide dielectric capacitor. However, platinum and silicon react <sup>with</sup> (to) each other, thereby <sup>to form</sup> platinum silicide <sup>[is formed]</sup> at their interface. Consequently, the electrical resistance of each electrode increases. Thus, the (conventional structure 1) allowing such a platinum electrode to come directly in contact with both <sup>the</sup> silicon substrate and polycrystalline silicon will not be suitable. Instead of (such the) conventional structure 1, therefore, another structure was proposed in 1989 IEEE Int. Solid-State Circuits Conf. Digest pp. 242-243. In <sup>this</sup> (the) structure, oxide dielectric capacitors are formed on <sup>a</sup> passivation layer. On the other hand, a MOS transistor is formed outside the capacitor area. And, a conductive wiring layer using aluminum, and the like is applied to connect the source or drain of the MOS transistor to the capacitor. In the case of this method that uses <sup>such a</sup> (this) conductive wiring layer, it is difficult to reduce the area of each memory cell, <sup>that</sup> so the method is not suitable for a memory <sup>which is</sup> (to be) highly integrated.

The official gazette of Unexamined Published Japanese Patent Application No. Hei-3-256358 disclosed a method for highly integrating a memory formed as follows; a semiconductor substrate provided with a MOS transistor formed thereon is coated with an insulating material; <sup>and</sup> <sub>on</sub> the

substrate an oxide dielectric capacitor is formed. In ~~the~~<sup>this</sup> method, contact holes are formed in the insulator and a conductive material is filled in the contact holes thereby to connect either ~~of~~<sup>the</sup> the source or the drain of the MOS transistor electrically to one of the two electrodes of the capacitor. Generally, polycrystalline silicon is used as the conductive material to be filled in the contact holes. This structure, however, could not avoid<sup>the</sup> occurrence of the above problems. In other words, ~~such~~<sup>the</sup> a structure that crystallizes oxide dielectrics directly on polycrystalline silicon (conventional structure 2; oxide dielectrics/polycrystalline silicon) oxidizes the interface between those materials, thereby forming a reaction insulating layer ~~there~~<sup>the formation of such a</sup>. On the other hand, in order to prevent ~~such the formed~~<sup>the</sup> reaction insulating layer, the (conventional structure 3; oxide dielectrics/platinum/polycrystalline silicon) is required. In this structure, platinum is inserted between polycrystalline silicon and oxide dielectrics to cope with the problem. This structure is substantially the same as the (conventional structure 1) in configuration. Platinum and polycrystalline silicon react ~~to~~<sup>with</sup> each other, thereby forming silicide. As a result, the electrical resistance of each electrode increases, ~~as well as~~<sup>and</sup> silicon diffuses into<sup>the</sup> platinum<sup>as well</sup>, causing a silicon oxide film to be formed on

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In order to solve those problems, the official gazettes of Unexamined Published Japanese Patent Application No. Hei-4-14862 and No. Hei-4-181766 disclosed

In addition to platinum, Ti, Ta, TiN, etc. used for electrode components, conductive oxides are also used as each electrode of an oxide dielectric capacitor. Such an example is reported in (Journal of Material Research, Vol.8 (1993), pp.12). This typical example <sup>represents a</sup> [is the] (fifth structure; oxide dielectrics/ruthenium oxide/<sup>SiO<sub>2</sub></sup>SiO<sub>2</sub>). If oxide dielectrics can be put directly in contact with ruthenium oxide, an advantage will be obtained <sup>in that</sup> [the] mechanical adhesive strength at the interface between oxide dielectrics and electrode increases more than when oxide dielectrics is put in contact with a completely different type metallic electrode. Such an increase of the mechanical adhesive strength between oxide dielectrics and <sup>the</sup> electrode

can improve the characteristics of the oxide dielectric capacitor, such as <sup>the</sup> polarization cycle, etc. In this example, the capacitor is formed on  $\text{SiO}_2$ . If the capacitor is formed on polycrystalline silicon, however, ruthenium oxide, which is an oxide, should not be put in contact directly with polycrystalline silicon for the same reasons as in the case of the (conventional structure 1) and the (conventional structure 3). And, in order to prevent such a direct contact, a noble metallic layer made of platinum, ruthenium, and the like should be formed between them. In this case, the (conventional structure 6: oxide dielectrics/ruthenium oxide/(platinum/ruthenium, etc.)/polycrystalline silicon) will be used suitably.

<sup>Summary</sup>  
[Disclosure] of the Invention

In the above related art, description was made <sup>for the</sup> conventional technology to be applied to memories to be integrated more highly by coating a MOS-transistor-formed-semiconductor substrate with an insulating material, <sup>and</sup> then forming an oxide dielectric capacitor thereon. As described above, the source or drain of the MOS transistor is connected electrically to one of the two electrodes of the capacitor through contact holes, which are generally filled with a conductive material consisting of polycrystalline silicon. And, the following two structures

are adopted for the conventional technology described above:

(Conventional Structure 4)

Oxide dielectrics/platinum/( Ti, Ta, TiN, etc.)/polycrystalline silicon

(Conventional Structure 6)

Oxide dielectrics/ruthenium oxide/(platinum, ruthenium, etc.)/polycrystalline silicon

Each of the above structures includes the following problems.

At first, the (conventional <sup>conventional</sup> a) structure 4) will be described. In order to crystallize oxide dielectrics, an oxidizing atmosphere at 500 °C or <sup>higher</sup> (over) is required. Under such a condition, however, oxygen diffuses along grain boundaries, etc. of platinum crystal grains, (thereby) <sup>to cause</sup> oxygen (reaches <sup>to reach</sup>) the anti-diffusion non-oxide conductive layer (Ti, Ta, TiN, etc.) to oxidize even <sup>that</sup> (the) layer. Consequently, the electrical resistance of the electrode itself increases. In order to avoid such a problem, the thickness of the platinum layer is increased. This method, however, makes it difficult to process the platinum layer, and <sup>results</sup> (result) in an increase <sup>in leakage</sup> of a leak current from the side wall of the capacitor. <sup>this is because</sup> (Because) the aspect ratio of the capacitor increases if the memory is highly integrated and <sup>a</sup> (the) fine capacitor is formed. And, this is why the (conventional



structure 4) cannot solve the conventional technology problems if Ti, Ta, TiN, etc. are used for an anti-interdiffusion layer.

Next, the (conventional structure 6) will be described. Also in this case, the ruthenium oxide layer is usually formed in an oxidizing atmosphere. Oxygen diffusion reaches up to polycrystalline silicon through the (platinum, ruthenium, etc.) layers, <sup>preventing</sup> disabling the (conventional structure 6) <sup>(from solving)</sup> to solve the conventional technology problems, including the one that an insulating layer is formed by (an) oxidation.

Such (the) conventional technology problems also occur not only from the <sup>specific</sup> materials <sup>described</sup> (shown) above (concretely), but also from layers consisting <sup>of</sup> (platinum, ruthenium, etc.) classified into noble metals, layers consisting of (Ti, Ta, TiN, etc.) classified into an anti-diffusion non-oxide conductive layer, and <sup>a</sup> (an) ruthenium oxide layer classified into a conductive oxide even when those materials are classified according to more general categories. In other words, both (conventional structure 4) and (conventional structure 6) are represented using more general material categories, that is, oxide dielectric/noble metal/anti-diffusion non-oxide dielectric layer/polycrystalline silicon in the (conventional structure 7) and oxide dielectric/conductor oxide/noble metal/polycrystalline

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silicon in the (conventional structure 8). The problems caused by each of the above layers <sup>which make up</sup> [composing] the above-described capacitor are summarized as follows.

At first, a noble metal layer will <sup>cause</sup> [arise] the following problems. (a) A noble metal layer will possibly cause a high resistance silicide to be formed if it comes in contact with silicon. (b) A noble metal layer will possibly become a diffusion path between chemical elements composing silicon, oxygen, and oxide. The problems <sup>which arise</sup> [arise] from oxide dielectric and conductive oxide layers will be as follows. (c) Such a layer will possibly oxidize <sup>the</sup> electrodes, thereby increasing <sup>the</sup> electrode resistance or insulating electrodes. Finally, an anti-diffusion non-oxide conductive layer will <sup>cause</sup> [arise] the following problem. (d) The layer will possibly be oxidized and its resistance will increase significantly.

✓ If the characteristics of both (conventional structure 7) and (conventional structure 8) are <sup>considered</sup> [noticed] here, the (conventional structure 9) will be <sup>considered based</sup> [reasoned] on <sup>the</sup> analogy of them. The (conventional structure 9) is obtained by compounding both of the structures simply. (Conventional Structure 9; oxide dielectric/conductive oxide/noble metal/anti-diffusion non-oxide conductive layer/polycrystalline silicon)

In this case, if an anti-diffusion non-oxide conductive layer is inserted, it is possible to solve one

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of the problems (a)(silicidation) and (b)(the diffusion of chemical elements composing silicon and oxides). However, the above problems (b), (c), and (d) related to oxygen diffusion and oxidation of electrodes remain unsolved just like the (conventional structure 4), since the conventional indispensable conditions for forming oxides in an oxidizing atmosphere are not improved [yet] at all.

In other words, the conventional technology cannot solve the problems such as oxygen diffusion and oxidation both caused by such oxides as oxide dielectrics and conductive oxides against such non-oxides as noble metals, anti-diffusion non-oxide conductive layers and polycrystalline silicon, not only when an oxide comes in contact with polycrystalline silicon directly, but also when an oxide comes in contact with polycrystalline silicon via a noble metal, as well as when an oxide comes in contact with an anti-diffusion non-oxide conductive layer via a noble metal.

As described above, in order to connect an oxide dielectric material to polycrystalline silicon electrically, an anti-oxidation layer must be formed between them. Conventionally, there <sup>has</sup> [have] been no effective anti-oxidation layer. Instead of such a layer, therefore, a metallic layer consisting of platinum, etc. <sup>has been</sup> [is] formed between them. Unfortunately, oxygen diffuses even at grain

boundaries of such a metallic layer, thereby reaching the anti-oxidation layer and probably resulting in oxidation of the layer. The thickness of the metallic layer was increased in some cases to compensate <sup>for this</sup> ~~the~~ disadvantage, but this resulted in an increase of the aspect ratio of the capacitor. This method will thus be <sup>undesirable</sup> ~~improper~~ for forming fine-structured memory cells. To solve this problem, therefore, a new and effective anti-diffusion or anti-oxidation layer has been awaited.

Under such ~~the~~ <sup>a</sup> circumstances, it is ~~the~~ <sup>a</sup> first object of the present invention to provide a semiconductor device, which can solve the above conventional technology problems. In order to achieve the first object, the semiconductor device of the present invention is provided with a fine-structured memory, which can be highly integrated using an oxide dielectric material (including ferroelectrics) for the insulator of the capacitor.

It is ~~the~~ <sup>a</sup> second object of the present invention to provide a method ~~for~~ <sup>of</sup> manufacturing such a semiconductor device.

In order to solve the above problems, the semiconductor device of the present invention, which includes a capacitor consisting of an oxide dielectric material, connects a semiconductor layer formed on the top surface of a semiconductor substrate or on a substrate to

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an oxide dielectric material via at least two layer areas, each of which consists of a conductive material different from the other. The materials of these two conductor areas (or material compositions) are combined thereby suppressing an increase of the electric resistance generated in the conventional technology in the anti-diffusion or anti-oxidation layer disposed between a semiconductor area and an oxide dielectric material area.

The semiconductor device of the present invention comprises <sup>a</sup>the first area consisting of a semiconductor material which is conductive (wiring layers and electrodes consisting of a semiconductor substrate or a semiconductor film); <sup>a</sup>the second area connected to the first area and consisting of <sup>a</sup>the first conductive material; <sup>a</sup>the third area connected to the second area and consisting of <sup>a</sup>the second conductive material; <sup>a</sup>the fourth area connected to the third area and consisting of an oxide dielectric material; and <sup>a</sup>the fifth area connected to the fourth area and consisting of a conductive material. Thus, the semiconductor device of the present invention has characteristics as follows in terms of the basic configuration; <sup>that is,</sup> the material composition at the interface adjacent to the second area in the first area is approximately equal to the average material composition of the first area, and the material composition at the interface adjacent to the first area in the second

area, as well as the material composition at the interface adjacent to the third area in the second area are approximately equal to the average material composition of the second area, respectively. As understood from these characteristics, the third and fifth areas <sup>(form)</sup> (compose) a capacitor via the fourth area. The oxide dielectric material <sup>which forms</sup> (composing) the fourth area may be replaced with a so-called ferroelectric material indicating a characteristic ( hysteresis) that a polarization value is changed differently between increasing and decreasing an applied electrical field.

The present invention is <sup>characterized</sup> (characterized) mainly as follows: The semiconductor is composed so that the first area has a material composition, which is approximately equal to the composition of the semiconductor material <sup>which forms</sup> (composing) the first area at the interface adjacent to the second area, and so that the second area has a material composition, which is approximately equal to the composition of the first conductive material at the interface adjacent to the first area and to the third area. In other words, the semiconductor device of the present invention is composed so as to make the material composition approximately homogeneous within the first and second <sup>areas</sup> (areas), respectively. And, there is no material (silicon oxide, metallic silicide, titanium oxide, etc. described above)

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that increases the electrical resistance in those areas. The materials that increase the electrical resistance as described above or the materials having an electrical insulating property actually (hereunder, to be referred to as a high resistance material) are formed around each interface between areas in a process in which the second to fourth areas are multi-stacked sequentially on the first area. On the contrary, according to the semiconductor device of the present invention, the first and second

conductive materials are selected properly so as to prevent the formation of a (formed) high-resistance material at the interface between the first and second areas, as well as at the interface between the second and third areas; and further, the first area is formed so that its material composition at the interface adjacent to the second areas becomes

approximately equal to the average material composition in the first area, and the second area is formed so that its material composition at the interface adjacent to the first area, as well as at the interface adjacent to the third area become approximately equal to the average material

composition in the second area. It will thus be understood clearly here that no high resistance materials are formed at the interface between the third and fourth areas because of the use of a noble metal of the (conventional structure 7) or the use of a conductive oxide of the (conventional

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structure 8) in the third area. In addition, an area (layer) consisting of a conductive material composed differently from the first and second conductive materials may be formed between the third and fourth areas, thereby to improve the electrical conductivity needed between the first and third areas or improve the conditions for forming <sup>an</sup> (the) oxide in the fourth area. In terms of the same aspect, an area (layer) consisting of a conductive material composed differently from the first and second conductive materials may be formed between the first and second areas. In short, what is important is that the second and third areas are connected to each other.

In an embodiment of the present invention, it is most important that the first and second conductive materials should be selected properly. There are two guidelines for selecting conductive materials. The object of the first guideline is as follows; two conductive materials are conductive oxides composed of the same chemical element and of the same framework of the crystal structure. The composition ratio of oxygen in the first conductive material is set lower than that in the second conductive material. In other words, the first conductive material is driven into <sup>an</sup> (the) oxygen deficiency <sup>state</sup>. The object of the second guideline is as follows; aluminum titanium nitride ( TiAlN) is used as the first conductive



### 1. Guideline 1 for selecting conductive materials

1. Guideline 1 for selecting conductive materials  
This guideline is <sup>directed</sup> ~~decided~~ to <sup>formation of</sup> ~~form~~ the second and third areas used as a double-layered conductive oxide layer, which can suppress oxygen diffusion and oxidation (the third object of the present invention) in order to achieve the first object of the present invention, as well as to provide a method <sup>of</sup> ~~for~~ manufacturing the double-layered conductive oxide layer, which can suppress oxygen diffusion and oxidation (the fourth object of the present invention) to achieve the second object of the present invention.

Here, description will be made first ~~(for)~~ the structure of a semiconductor device that uses a capacitor consisting of an oxide dielectric material, especially the structure of a semiconductor device composed of a double-layered

Next, description will be made <sup>concerning</sup> for a semiconductor device that will achieve the first object of the present invention described above. The semiconductor device of the present invention includes a capacitor composed of oxide dielectrics used as an insulator. Fig.1 shows a schematic diagram of such a capacitor composed of oxide dielectrics.

Next, description will be made for a semiconductor device that will achieve the first object of the present invention described above. The semiconductor device of the present invention includes a capacitor composed of oxide dielectrics used as an insulator. Fig.1 shows a schematic diagram of such a capacitor composed of oxide dielectrics.

Fig.1 does not show a detailed structure of the capacitor of the semiconductor device, which is composed of oxide dielectrics. It shows multi-stacked layers of the capacitor in order to simplify the structure. An oxide dielectric capacitor consists of a lower electrode layer 11 formed on a substrate (shown only in the direction of the substrate side 10 in Fig.1), an oxide dielectric layer 16 formed on the layer 11, and an upper electrode layer 17 formed on the layer 16. The lower electrode layer 11 includes a conductive oxide layer 12 and this conductive oxide layer 12 consists of two adjacent layers 14 and 15, which have the same crystal structure and consist of the same chemical elements. Each of the layers 14 and 15 has a composition ratio of oxygen different from the other. In other words, only the conductive oxide layer 14 positioned at the substrate side <sup>has an</sup> [includes] oxygen deficiency. These conductive oxide layers 14 and 15 correspond to the second and third areas described above.

In such a semiconductor device, the lower electrode layer 11 is connected electrically to the source area or the drain area of a MOS transistor formed on the substrate via the lower electrode layer component 13 including at least more than one layer formed closer to the substrate than the conductive oxide layer 14 with oxygen deficiency. Hereunder, an example of this lower electrode layer

component 13 will be described in detail with reference to Figs. 2, 3 and 4.

Fig. 2 shows a configuration of an oxide dielectric capacitor when the lower electrode layer component 13 which is positioned closer to the substrate than the conductive oxide layer 14 with oxygen deficiency in Fig. 1 consists of a conductive polycrystalline silicon layer 20. The conductive polycrystalline silicon layer 20 mentioned here corresponds to the first area described above. A structure in which an oxide comes in contact with silicon directly is not favorable as described above with respect to the conventional structure, since silicon is oxidized unavoidably under typically necessary conditions for crystallizing the oxide, that is, at 500 °C or <sup>higher</sup> (over) in an oxidizing atmosphere. According to the present invention, however, the conductive oxide layer 14 with oxygen deficiency is formed <sup>to</sup> (as an) adjacent (layer of) the polycrystalline silicon layer 20, so that the structure as shown in Fig. 2 is realized. The characteristics of the double-layered conductive oxide layer 12 including the conductive oxide layer 14 with oxygen deficiency will be described later.

Fig. 3 shows <sup>the</sup> a) configuration of an oxide dielectric capacitor when the component 13 <sup>forming</sup> (composing) the lower electrode layer consists of a non-oxide conductive layer for

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anti-diffusion 30 and a conductive polycrystalline silicon layer 20. The lower electrode layer is positioned closer to the substrate side than the conductive oxide material 14 with oxygen deficiency as shown in Fig.1. The anti-diffusion non-oxide conductive layer 30 corresponds to a layer formed between the first and second areas described above. The conventional technologies cannot avoid oxidation of the anti-diffusion non-oxide conductive layer caused by the oxygen that diffuses at grain boundaries in a noble metal at 500 °C or over in an oxidizing atmosphere, even when a noble metal is used to separate the oxide from the anti-diffusion non-oxide conductive layer as seen in the (conventional structure 7). Those are typical conditions needed to crystallize an oxide. Thus, such a structure <sup>places</sup> (as) <sup>which</sup> (allowing) an oxide (to be put) in contact directly with the anti-diffusion non-oxide conductive layer 30 as described above is not suitable. According to the present invention, however, <sup>when</sup> <sup>positioned</sup> a conductive oxide layer 14 with oxygen deficiency is adjacent to the anti-diffusion non-oxide conductive layer 30, the structure as shown in Fig.3 is (thus) realized. The characteristics of the double-layered conductive oxide layer 12 including the conductive oxide layer 14 with oxygen deficiency will be described later.

Fig.4 shows <sup>the</sup> (a) configuration of an oxide dielectric capacitor when the component 13 <sup>forming</sup> (composing) the lower

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electrode layer positioned closer to the substrate side than the conductive oxide material 14 with oxygen deficiency shown in Fig.1 consists of a metallic layer 40, an anti-diffusion non-oxide conductive layer 30, and a conductive polycrystalline silicon layer 20. The metallic layer 40 and the anti-diffusion non-oxide conductive layer 30 correspond to a layer formed between the first and second areas described above [respectively]. The conventional technologies cannot avoid oxidization of the anti-diffusion non-oxide conductive layer, which <sup>is</sup> caused by (the) oxygen diffusion through the metallic layer 40 at 500 °C or (over) <sup>drift</sup> in an oxidizing atmosphere, which are typical conditions needed to crystallize oxides. In order to suppress such [the] oxidization, therefore, the thickness of the metallic layer 40 must be increased as described above. According to the present invention, however, a conductive oxide layer 14 with oxygen deficiency <sup>positioned</sup> is adjacent to the metallic layer 40. The structure as shown in Fig.4 is thus realized regardless [however] <sup>of how</sup> thin the metallic layer 40 is. The characteristics of the double-layered conductive oxide layer 12 including the conductive oxide layer 14 with oxygen deficiency will be described later.

A noble metal highly resistant to oxidization will be considered as a candidate for forming such <sup>a</sup> (the) metallic layer. Concretely, among noble metals, at least one of the

following noble metal elements will be suitable; platinum which is highly resistant to oxidization, ruthenium, or iridium composed of the same element as the noble metal element included in the conductive oxide layer to be described later.

Hereunder, materials suitable for the anti-diffusion non-oxide conductive layer will be described. Necessary conditions to satisfy the requirements of the anti-diffusion non-oxide conductive layer 30 are conductivity at first, then resistance to oxidization, and resistance to reaction with silicon. Compounds to be considered as candidates for the anti-diffusion non-oxide conductive layer 30 are nitride, silicide, boride, and carbide. The anti-reaction to silicon is stable in any of those compounds. Any of them can be used with no problem. Of course, if the object semiconductor device is annealed at 1000 °C or <sup>higher</sup> ~~over~~, the elements of any of those compounds will react to silicon, thereby forming reaction products of high resistance or insulation properties possibly. However, a back-end process including <sup>the formation</sup> ~~(forming)~~ of an oxide dielectric capacitor for a semiconductor device will require only a heating condition of 800 °C at <sup>the</sup> highest for a few minutes, which will not form such reaction products caused by mutual diffusion of elements. The reaction to silicon can thus be neglected. As for the resistance to oxidization, there

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will arise no problem in the case <sup>where</sup> (of that) the conductive oxide layer with oxygen deficiency of the double-layered conductive oxide layer is put adjacent to the anti-diffusion non-oxide conductive layer (Fig. 3). As <sup>will</sup> to be described later, this is because the conductive oxide layer with oxygen deficiency must be formed in a non-oxidizing atmosphere and the conductive oxide layer with oxygen deficiency functions as an obstacle in the oxygen diffusion path. In addition, since the conductive oxide layer with oxygen deficiency is over-stacked on the anti-diffusion non-oxide conductive layer 30 with a metallic layer therebetween (Fig. 4), the anti-diffusion non-oxide conductive layer 30 is separated farther from the oxide layer. In addition, forming a metallic layer adjacent to the anti-diffusion non-oxide conductive layer <sup>has</sup> never <sup>caused</sup> arisen any problem conventionally.

Hereunder, a concrete example of the anti-diffusion non-oxide conductive layer will be described. A nitride will be suitable if it includes at least one of such metal types <sup>as</sup> Ti, Ta, Zr, Nb, V, and W, since it becomes very conductive. In addition <sup>to</sup> those materials, <sup>a</sup> silicide such as Ti, <sup>a</sup> boride such as La, <sup>and a</sup> carbide such as Ti, will also be suitable.

Next, materials suitable for an oxide dielectric layer will be described. Ferroelectric materials are also



oxide dielectric materials, of course. There is no reason <sup>to</sup> (that must) limit the materials. There are some well-known materials as shown below, however. Typical examples of oxide dielectrics of which <sup>the</sup> center element is titanium are; lead zirconate titanate obtained by replacing part or (whole) <sup>all</sup> of the titanium with zirconium, lead barium zirconate titanate obtained by replacing part or (whole) <sup>all</sup> of the lead with barium, <sup>and</sup> barium strontium titanate including only alkaline earthmetals, etc. As typical examples of bismuth-system dielectrics composed in a layered structure, there are bismuth layered dielectrics such as  $\left[ \text{Bi} \begin{smallmatrix} \text{Bi}_4\text{Ti}_3\text{O}_{12} \\ \text{SrBi}_2\text{Ta}_2\text{O}_9 \end{smallmatrix} \right]_{0.9}$  etc.

In addition to those well-known oxide dielectrics and oxide ferroelectrics, [as well as] new oxide dielectrics and oxide ferroelectrics to be discovered in the future, etc. are usable as the oxide dielectric layer described above.

Next, the characteristics of the double-layered conductive oxide layer 12 including a conductive oxide layer with oxygen deficiency will be described. [since] <sup>as</sup> mentioned (so) in the description of the structures shown in Figs. 2 to 4. Here, description will be made for the structure, function, and manufacturing method of the double-layered conductive oxide layer in order to achieve the method (for) manufacturing the semiconductor device, which is the second object of the present invention, the function of the

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double-layered conductive oxide layer that can suppress oxygen diffusion and oxidation, which is the third object of the present invention, and the method <sup>of</sup> manufacturing the double-layered conductive oxide layer, which is the fourth object of the present invention.

As described above, it is <sup>the</sup> oxidizing of the anti-diffusion non-oxide conductive layer and polycrystalline silicon that are already stacked <sup>that creates</sup> (to become) a problem when <sup>(in)</sup> forming an oxide layer for dielectrics and electrodes. The oxidation is caused by an oxidizing atmosphere, which is indispensable for forming oxide layers. What must be emphasized here <sup>is</sup> that <sup>the</sup> <sup>due to a</sup> problem is not <sup>the</sup> reaction between oxide and silicon or between oxide and an anti-diffusion non-oxide conductive layer. In terms of the standard Gibbs free energy, oxides composed of alkali earth metals such as Sr and Ca, and transition elements such as Ru and Ti are more stable than oxidation of Si. An anti-diffusion non-oxide conductive layer composed of nitride, silicide, boride, and carbide of transition metals cannot be expected to be oxidized through reaction <sup>with</sup> (to) an oxide in terms of the free energy. If anything, they are all oxidized by an oxidizing active gas in the atmosphere needed for forming an oxide layer. Consequently, the present inventor has concluded that the above problems can be solved if an oxide layer is formed in a non-oxidizing atmosphere in expectation that <sup>the</sup>

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other elements <sup>which make up</sup> (composing) the semiconductor device of the present invention would not be oxidized.

Generally, the oxide dielectrics (including ferroelectrics) forming an oxide dielectric capacitor and oxide films such as conductive oxide electrodes are formed in an oxidizing atmosphere. This is mainly because oxides are unstable chemically in a non-oxidizing atmosphere and no oxide film is formed or even when it is formed, its characteristics are not satisfactory. Because the vapor pressure of typical elements is high, film formation under an insufficient oxidizing condition surely causes selective evaporation, that is, a variation in composition in oxide ferroelectrics including group-4 and group-5 typical elements such as lead and bismuth. At the same time, since decomposed products other than object compounds also come to be mixed, the ferroelectric properties are degraded significantly. In addition, the non-oxidizing atmosphere causes oxygen deficiency in the object compound. In the case of oxide dielectrics including group-4 transition elements such as titanium and zirconium, oxygen deficiency will cause the dielectric constant to be lowered, <sup>which</sup> (as well as) causes a leakage <sup>to flow</sup> current. Consequently, it is not realistic to form an oxide dielectric film in a non-oxidizing atmosphere.

As for another oxide for forming oxide dielectric capacitors, that is, conductive oxide electrodes, it was

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expected that films could be formed in a non-oxidizing atmosphere as long as <sup>this</sup> (it) does not affect the characteristics of electrodes or the object semiconductor device even when oxygen deficiency was introduced into compounds and simultaneously decomposed products were mixed while the films were formed in a non-oxidizing atmosphere. In other words, the oxygen deficiency reduces or increases the charge density, as well as changes its mobility, thereby increasing its resistivity. However, no problem arises as long as the resistivity required for the electrode layer is secured.

Forming (of) films in a non-oxidizing atmosphere will also <sup>create</sup> (arise) no problem as long as the resistance required for the electrode layer is secured even when the resistivity is increased by coexistence of some decomposed products.

The component 13 of the lower electrode layer adjacent to the conductive oxide layer 12 in Fig.1, corresponds to the polycrystalline silicon layer 20 in Fig.2, the anti-diffusion non-oxide conductive layer 30 in Fig.3, and the anti-diffusion non-oxide conductive layer 30 through the metallic layer 40 in Fig.4, respectively. In order to prevent those layers from <sup>oxidizing</sup> (oxidation), the present inventor thought it would be better to form the side 14 at which the conductive oxide layer 12 was adjacent to the component 13 (20, 30 and 40) of the lower electrode layer in a non-oxidizing atmosphere. The layer 14 was thus formed up to

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a certain thickness. And, the rest <sup>of 14</sup> layer 15 of the conductive oxide layer 12 was formed continuously in an oxidizing atmosphere by changing the oxidizing activity of only the film deposition conditions, such as the oxygen pressure and the type of the oxidizing gas. In other words, the conductive oxide layer 12 is composed <sup>two</sup> of adjacent <sup>formed to have</sup> [two] layers 14 and 15, and these two layers are <sup>formed in</sup> [composed in] the same crystal structure and <sup>of</sup> [with] the same element, but differently from each other in the composition ratio of oxygen. Only the layer 14 of the two adjacent layers includes <sup>an</sup> oxygen deficiency. The layer 14 is positioned at the [composed] component 13 side of the lower electrode layer, that is, at the substrate side.

Since the conductive oxide layer 14 is <sup>formed</sup> [for] med] in a non-oxidizing atmosphere, the adjacent lower electrode layer component 13 (polycrystalline silicon layer 20, the anti-diffusion non-oxide conductive layer 30, and the metallic layer 40) <sup>is</sup> [are] not oxidized. The conductive oxide layer 14 with oxygen deficiency, after it is formed once, is stable in terms of the standard Gibbs free energy. Then, the component 13 (20, 30, and 40) of the lower electrode layer is also not oxidized. And, as shown in Fig. 4, even when a metallic layer 40 is inserted therebetween, the anti-diffusion non-oxide conductive layer 30 is never [be]

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oxidized by oxygen diffusion, <sup>that</sup> so the thickness can be <sup>reduced</sup> thinned as much as possible.

After the <sup>formation</sup> forming of the conductive oxide layer 14 with oxygen deficiency, the conductive oxide layer 15 and the oxide dielectric layer 16 are formed in an oxidizing atmosphere. If the conductive oxide layer 14 includes <sup>an</sup> oxygen deficiency, the layer 14 acts as a diffusion buffer layer against oxygen even when those layers 15 and 16 are formed in an oxidizing atmosphere. In other words, even when the surface of the conductive oxide layer 14 with oxygen deficiency is exposed to an oxidizing gas, the layer 14 acts as a buffer layer against the oxygen diffusion ions, <sup>as well</sup> (as well) <sup>and</sup> (as) captures diffusing oxygen ions. Since the conductive oxide layer 14 itself is stable in terms of the standard Gibbs free energy, the layer 14 acts as an anti-oxidation layer for the component 13 (20, 30, and 40) of the lower electrode layer.

Consequently, the double-layered conductive oxide layer including a conductive oxide layer with oxygen deficiency, which is formed in a non-oxidizing atmosphere, acts as an excellent oxidation resistant film and an oxygen diffusion barrier layer.

The thickness of the conductive oxide layer 14 (with oxygen deficiency), which is formed in a non-oxidizing atmosphere, should preferably be 10nm or larger. The reason

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is that the component 13 (20, 30, and 40) of the lower electrode layer is completely covered so as to be prevented from oxidizing when the conductive oxide layer 15 and the oxide dielectric layer 16 are formed in an oxidizing atmosphere. The upper limit is not determined specially for the thickness. All of the conductive oxide layers 12 may be composed of a conductive oxide layer 14 (with oxygen deficiency) which is formed in a non-oxidizing atmosphere. In this case, however, since the following oxide dielectric layer 16 is formed off course in an oxidizing atmosphere, the interface of conductive oxide layer 14 adjacent to the oxide dielectric layer 16 is oxidized. Consequently, a thin layer 15 is formed at the interface. The double-layered conductive oxide layer 12 can thus be formed.

Hereunder, a non-oxidizing atmosphere will be described with respect to a method for manufacturing the double-layered conductive oxide layer. <sup>One type of</sup> [A certain] non-oxidizing atmosphere is an atmosphere including a hydrogen gas and a reducing gas. In such a reducing atmosphere, however, much oxygen is <sup>taken out</sup> [takeout] while an oxide film is grown in the film deposition process. The film is thus possibly reduced to a <sup>metal</sup> [metal]. A milder non-oxidizing atmosphere is an inactive gas atmosphere that uses inert <sup>gases</sup> [gasses] such as argon and helium, or a vacuum into which none of oxidizing gases such as oxygen ( $O_2$ ), nitride monoxide ( $N_2O$ ), nitric

Concretely, the condition of a non-oxidizing atmosphere depends on respective film deposition methods with which a conductive oxide layer is formed. At first, when an oxide film is formed in an inert gas or inactive gas atmosphere or in a vacuum, no oxygen is supplied from the growth environment. The film deposition source must include oxygen. This film deposition category includes a sputtering

Concretely, the condition of a non-oxidizing atmosphere depends on respective film deposition methods with which a conductive oxide layer is formed. At first, when an oxide film is formed in an inert gas or inactive gas atmosphere or in a vacuum, no oxygen is supplied from the growth environment. The film deposition source must include oxygen. This film deposition category includes a sputtering



method, a laser deposition method, both of which use a sintered oxide target, an electron beam evaporation method that uses an oxide evaporation source, etc. Since the sputtering method needs a discharge gas, introduction of <sup>(an)</sup> argon (Ar) gas of 3N (99.9%) or up in purity by a few mTorr to a few tens of mTorr will do. It should be avoided, however, to use a gas of low purity, since such a gas brings <sup>about</sup> an unexpected result such as unstable discharge, precipitation of impurity phases, etc. The laser deposition method can form oxide films in a vacuum. Of course, no problem will occur if any of <sup>the</sup> inert <sup>gases</sup> (gasses) are used just like in the sputtering method, but it makes no sense principally. Films can also be formed by <sup>an</sup> electron beam deposition method that uses an oxide evaporation source. The vacuum mentioned here is a state achieved by any of <sup>the known</sup> evacuation devices without introducing oxidizing gases such as oxygen, nitrogen monoxide, nitrogen dioxide, ozone, etc. intentionally. The pressure should preferably be  $1\mu\text{Torr}$  or under in terms of the non-oxidizing atmosphere in both laser deposition and electron beam deposition methods.

Each of the film deposition methods described above can be applied to form an oxide film on the anti-diffusion non-oxide conductive layer (including a case when the layer is formed via a metallic layer) in a weak oxidizing atmosphere including oxidizing gases such as oxygen,

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nitrogen monoxide, nitrogen dioxide, ozone, etc. slightly. The sputtering method is just required to include an oxidizing gas used as a discharge gas. The laser deposition method is just required to include an oxidizing gas. The electron beam deposition method, when used in a vacuum, can use only an oxide as an evaporation source. When it is used in a weak oxidizing atmosphere, however, it can also use a metal evaporation source. Consequently, the method can use a heater such as an effusion cell (K cell) as a heating source in addition to the electron beam. The pressure should preferably be  $10 \mu\text{Torr}$  or lower in total pressure or partial pressure of the oxidizing gas in use in terms of the non-oxidizing atmosphere in any of the sputtering method, the laser deposition method, and other deposition methods that use an electron beam and a heater.

✓ On the basis of the ideas described above, the following results have been obtained when (in) checking (of) the conductive oxides that can satisfy the conditions with respect to the rutile structure, the perovskite structure, and the  $\text{ReO}_3$  structure in which many conductive oxides are known: (a) The resistivity in the room temperature is  $0.01 \Omega\text{cm}$  or lower. (b) Possible to be stabilized in a non-oxidizing atmosphere and under typical conditions (oxygen pressure of  $1 \mu\text{Torr}$  and temperature of  $700^\circ\text{C}$ ).

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In order to satisfy the above requirement (b), it is not desirable that a conductive oxide is composed of <sup>a</sup> multi-valent ion, <sup>such as a</sup> (which are) positive center cation. Consequently, conductive oxides including Cr, Mn, Fe, Co, Ni, Cu, and V are excluded.

There are two conductive oxides that crystallized in the rutile structure:  $[RuO_2]$  and  $[IrO_2]$

There are three conductive oxides that crystallized in the perovskite structure:  $CaRuO_3$  and  $SrRuO_3$  whose center element is Ru (ruthenium), and  $(La, Sr)TiO_3$  in which part of Sr of  $[SrTiO_3]$   <sup>$SrTiO_3$</sup>  whose center element is Ti (Titanium) is replaced with La by over 0.5 weight % to 4.0 weight % (included) in quantity.

$ReO_3$  is another conductive oxide that takes the  $ReO_3$  structure.

When forming a conductive oxide in a non-oxidizing atmosphere, oxygen deficiency is introduced as described above. In the thermal equilibrium state, only <sup>a</sup> slight oxygen deficiency of 0.1% or lower is introduced as a point defect, but film deposition is often <sup>carried out</sup> (made) in a non-equilibrium state. Thus, an extra oxygen defect is easily frozen excessively unlike in the thermal equilibrium state. It is very difficult, however, even with the current analysis technique to measure an oxygen defect concentration specific to films. Actually, it is impossible to define an

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oxygen defect concentration with an accurate value. On the other hand, no remarkable impurity was identified when a crystal structure of the film which was deposited in a non-oxidizing atmosphere was analyzed by an X-ray diffractometer. The stoichiometry of cations could be confirmed in the compositional analysis using the ICPS (Inductivity-Coupled Plasma Spectroscopy). At this time, <sup>compared to</sup> the resistivity increased by almost 10% in maximum ~~(than in)~~ deposition of the same films in an oxidizing atmosphere. This suggests that an oxygen deficiency is surely introduced.

A film formed in a non-oxidizing atmosphere will be defined concretely as follows on a condition that the permissible oxygen deficiency allows an objective structure to be kept stable. For the rutile structure, it is defined that an oxygen deficiency  $x$  is larger than 0 and smaller than a value that enables the rutile structure to be kept stable in the chemical formula  $MO_{2-x}$  with oxygen deficiency in which both Ru and Ir transition elements are represented by M. For the perovskite structure, it is defined that the oxygen deficiency  $x$  is larger than 0 and smaller than a value (upper limit value) that enables the perovskite structure to be kept stable in the chemical formula  $AMO_{3-x}$  with oxygen deficiency in which both Ru and Ti transition elements are represented by M, and Ca, Sr, and La elements are represented

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by A, respectively. At this time, even when an anti-site defect is introduced between cations due to the introduced oxygen deficiency, <sup>such that the</sup> ~~thereby a~~ lattice constant becomes larger than the standard bulk value, the basic framework is judged to be still within the category of the perovskite structure. For the  $\text{ReO}_3$  structure, it is defined that the oxygen deficiency  $x$  is larger than 0 and smaller than a value that enables the  $\left( \begin{smallmatrix} \text{ReO}_3 \\ \text{MO}_{3-x} \end{smallmatrix} \right)$  structure to be kept stable in the chemical formula  $\left( \text{MO} \right)_{3-x}$  with oxygen deficiency.

The introduction of oxygen deficiency causes the resistivity of the conductive oxide to be increased by almost 10% in maximum, but the conductive oxide is kept low in resistivity <sup>sufficient</sup> ~~(enough)~~ to be used as electrodes. For example, the resistivity was increased by almost 10% in  $\text{SrRuO}_{3-x}$ , but the resistivity was as small as a few  $\text{m}\Omega\text{cm}$  as an absolute value. In  $\left[ \text{IrO}_{2-x}, \text{RuO}_{2-x}, \text{and ReO}_{3-x} \right]$  the resistivity was increased only to about double in maximum. In other words, it was confirmed that the conductive oxides could keep a resistivity <sup>sufficient</sup> ~~(enough)~~ to be used for electrodes even when the conductive oxides described above were formed in a non-oxidizing atmosphere.

A possibility of coexistence of decomposed products was as described above when a conductive oxide was formed in a non-oxidizing atmosphere. Both  $\text{RuO}_2$  and  $\text{IrO}_2$  in rutile structures, as well as the  $\text{ReO}_3$  are a monoxide respectively

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and each of those structures includes only one type of transition element. <sup>there</sup> (1) is thus no fear that they are decomposed thereby to produce other compounds. On the other hand, the perovskite structure expressed by  $\text{AMO}_3$  is a complex oxide which consists of an element M consisting of transition elements and an element A consisting mainly of alkaline-earth metals. It is thus possible that decomposed products coexist at a high temperature of about  $700^\circ\text{C}$  in a non-oxidizing atmosphere. Actually, when Ca was included as an alkaline-earth metal, it was confirmed by an X-ray diffractometer that about a few %  $\text{CaO}$  existed as a decomposed product. Even when Sr was included,  $\text{SrO}$  was observed as a decomposed product in a stronger non-oxidizing atmosphere, that is, at a higher temperature and at a lower pressure. In any <sup>of the</sup> cases described above, therefore, it was recognized that nothing affected the resistivity (in the <sup>at</sup> room temperature. It was concluded from this result that (highly) resistant decomposed products were distributed and coexisted in a conductive oxide, so that a current was <sup>caused to flow</sup> (flowed) in a lower objective conductive oxide.

At a lower temperature than (the) room temperature, a metallic conduction was observed, where the resistivity was decreased as the temperature was decreased if there was no decomposed product. If decomposed products coexisted, a conduction that caused the resistivity to be increased was

observed. It was concluded from this result that the increase of the resistivity was caused by the conduction characteristics of decomposed products segregated along grain boundaries in a <sup>microscopic</sup> [microscopic] fashion.

In any <sup>of the</sup> cases described above, at ~~(the)~~ room temperature or above, the increase of the resistivity caused by coexistence of decomposed products was within an allowable range for conductive oxide layers or semiconductor devices that used conductive oxide layers. In other words, each of <sup>the</sup> conductive oxides that take the perovskite structure may be a mixed phase of  $\text{CaRuO}_3$ ,  $\text{SrRuO}_3$ , and  $(\text{La}, \text{Sr})\text{TiO}_3$  in which a part of Sr of  $\text{SrTiO}_3$  is replaced with La by over 0.5 to 4.0 weight% (included), and an alkaline earthmetal oxide  $\text{CaO}$  or  $\text{SrO}$  composing the subject oxide.

Description has been made <sup>so</sup> [s] <sup>of a</sup> ~~of a~~ far ~~for the~~ means for achieving the first object of the present invention, that is the characteristics of a semiconductor device, using oxide dielectrics as a capacitor insulator and a double-layered conductive oxide layer as an electrode element, as well as for the means for achieving the second object of the present invention, that is, a method ~~for~~ forming the double-layered conductive oxide layer, selected from the methods ~~for~~ manufacturing such a semiconductor device, and for the means for achieving the third object of the present invention, that is, the characteristics of the double-

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layered conductive oxide layer that can suppress oxygen diffusion and oxidation, and for the means for achieving the fourth object of the present invention, that is, a method <sup>for</sup> forming the double-layered conductive oxide layer.

Finally, description will be made <sup>for the</sup> means for achieving the second object of the present invention, that is, a method <sup>for</sup> manufacturing such a semiconductor device. The method <sup>for</sup> manufacturing the semiconductor device of the present invention includes processes for forming a lower electrode layer on a substrate as described above with reference to Figs.1 to 4. The lower electrode layer consists of a polycrystalline silicon layer, a non-oxide conductive layer for anti-diffusion, a metallic layer, and a double-layered conductive oxide layer. Usually, a polycrystalline silicon layer is formed using <sup>the</sup> chemical vapor deposition. The non-oxide conductive layer for anti-diffusion is formed using <sup>the</sup> sputtering method, <sup>the</sup> vacuum deposition method, and <sup>the</sup> CVD method. The metallic layer is formed using <sup>the</sup> sputtering method. However, the methods for forming those layers are just examples and they are not limited for modification specially. How to form the double-layered conductive oxide layer is as described <sup>above</sup> in detail. The compound of each layer for composing the lower electrode is also as described above in detail.

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In order to form an oxide dielectric capacitor, <sup>in which</sup> [so that] <sup>any</sup> its oxide dielectric layer <sup>positioned</sup> is between the upper and lower electrode layers, an oxide dielectric layer is formed on this lower electrode layer, then the upper electrode layer is formed on the oxide dielectric layer. Concrete compounds used for forming the oxide dielectric layer are as described above in detail. The sol-gel method with use of alkoxide, the vacuum <sup>method</sup> deposition method, the chemical vapor deposition, the sputtering method, etc. can be used to form <sup>to</sup> the oxide dielectric layer. The methods are not limited only <sup>identified</sup> those specially. The upper electrode layer should preferably be formed with the same conductive oxide as that of the lower electrode layer if the symmetry of the current - voltage characteristics of the dielectric capacitor, as well as the symmetry of the polarization hysteresis curve of the ferroelectric capacitor are considered to be important. However, the semiconductor device will work as expected even if the conductive oxide and a noble metal such as platinum, ruthenium, and iridium are different between the upper and lower electrode layers. The upper electrode layer can be formed by any of sputtering, vacuum deposition, sol-gel, and chemical vapor deposition methods. The film deposition method is not limited only to those specially <sup>provided</sup> even when a noble metal is used for forming the upper electrode layer.

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Before the oxide dielectric capacitor, that is, the lower electrode layer is formed, part of a MOS transistor is formed on the substrate. The source area or the drain area of the MOS transistor is connected electrically to the lower electrode layer through the conductive material filled in the contact holes formed through the insulator, which covers the semiconductor substrate on which the MOS transistor itself is formed. Polycrystalline silicon formed using the chemical vapor deposition <sup>method</sup> is often used as the conductive material filled in these contact holes. The polycrystalline silicon deposition <sup>method</sup> and the filling material are not limited only those specially <sup>mentioned</sup>.

## 2. Guideline 2 for Selecting Conductive Materials

This guideline is determined to achieve the first and second objects of the present invention, especially on the basis of the configuration of (the conventional technology 7).

In order to achieve the first object of the present invention, the semiconductor device of the present invention is provided with an oxide dielectric capacitors formed on a semiconductor substrate. The capacitor consists of a lower electrode layer including an aluminum titanium nitride layer, an oxide dielectric layer formed on the aluminum titanium nitride layer, and an upper electrode layer formed on the oxide dielectric layer. Figs.5 and 6

show two typical cross sectional views of the lower electrode layer. Figs. 5 and 6 do not show any detailed structure of the oxide dielectric capacitor provided in the semiconductor device of the present invention, but they show simplified views of how each layer of the capacitor is stacked.

In Fig. 5, the lower electrode layer 11 consists of the aluminum titanium nitride layer 50 formed on the polycrystalline silicon layer 20, and the metallic layer 40 formed [further] on the layer 50. The conductive polycrystalline silicon layer 20 corresponds to the first area described above in the concept of the semiconductor device. The aluminum titanium nitride layer 50 corresponds to the second area described above in the concept of the semiconductor device. The metallic layer 40 corresponds to the third area described above in the concept of the semiconductor device. In Fig. 6, a conductive oxide layer 60 is stacked on the component of the lower electrode layer 11 shown in Fig. 5. This conductive oxide layer 60 corresponds to an area provided between the third and fourth areas described above in the concept of the semiconductor device.

The lower electrode layer 11 is also connected electrically to a predetermined area of the semiconductor

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element formed on the substrate, for example, the source or drain area of a MOS transistor.

Hereunder, the function of the aluminum titanium nitride layer 50 used for preventing <sup>oxygen</sup> (oxygen) diffusion and oxidation will be described. As <sup>provided</sup> (described) in the conventional technologies, the titanium nitride layer used as a layer for preventing oxygen diffusion and oxidation, which <sup>has</sup> (have) been examined so far, is weak in anti-reaction to oxygen. And, in order to compensate this weak point of the titanium nitride layer, it is indispensable to put a metallic layer made of platinum, etc. therebetween. A platinum <sup>layer</sup> of about 200nm in thickness is also needed to secure a time of oxygen diffusion at grain boundaries in <sup>the</sup> platinum. On the other hand, the titanium nitride layer still has <sup>an</sup> attraction, since it acts to prevent oxidation to a certain level while it keeps a high conductivity. This is why aluminum is added to titanium nitride to obtain a remarkable resistance to oxidation. The resistance was found as a result of examination for the possibility of improvement of the resistance to oxidation by adding the second metallic element to titanium nitride.

The reaction of a <sup>nitride</sup> (nitride) to oxidation, thereby to be changed into an oxide, is considered to be a reaction (that) <sup>to</sup> substitute oxygen with nitrogen in the nitride. In other words, it may be considered that the height of the energy

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barrier between the nitride and the oxide dominates this substitution qualitatively. In the aluminum titanium nitride obtained by the present invention, the improvement of the anti-reaction to oxygen is considered to be caused by this heightened energy barrier. Regardless of this chemical <sup>(background)</sup> ~~back ground~~, however, it was found that the aluminum titanium nitride could function <sup>sufficiently</sup> ~~enough~~ as an anti-oxidizing layer if part of <sup>the</sup> titanium in the titanium nitride is replaced with aluminum. In terms of this anti-oxidizing property, if the chemical formula of the aluminum titanium nitride was expressed by  $(\text{Ti}_{1-x}\text{Al}_x)_{1-y}\text{N}_y$ , x should preferably be 0.2 or above and y should preferably be 0.4 or above. If x is smaller than 0.2, the anti-oxidizing property is not improved at all. If y is smaller than 0.4,  $\text{TiO}_2$  produced by oxidation is observed in an X-ray diffraction measurement.

Aluminum nitride is a high resistant material. If part of <sup>the</sup> titanium is replaced with aluminum, the resistivity increases. If such aluminum titanium is to be used for each electrode of a semiconductor device, the resistivity should preferably be  $10\text{m}\Omega\text{cm}$  or under. Consequently, if aluminum titanium nitride is represented by a chemical formula of  $(\text{Ti}_{1-x}\text{Al}_x)_{1-y}\text{N}_y$ , x should preferably be 0.5 or below and y should preferably be between 0.4 and 0.6. If an impurity phase is precipitated, the material becomes <sup>non-homogeneous</sup> ~~(inhomogeneous)~~.

in the electrode, <sup>and</sup> thereby <sup>this</sup> forming of fine-integrated memory cells is disabled. In order to avoid this, the x value should preferably be 0.6 or below and the y value should preferably be 0.2 or above, and 0.6 or below.

In conclusion, the x value should preferably be 0.2 or above, and 0.5 or below and the y value should preferably be 0.4 or above, and 0.6 or below in the aluminum titanium nitride expressed by a chemical formula of  $(\text{Ti}_{1-x}\text{Al}_x)_{1-y}\text{N}_y$ .

Another requirement for the aluminum titanium nitride layer, that is, the property of anti-diffusion is expected to be equivalent to that in the titanium nitride layer, since the structure of titanium nitride which is a mother compound is maintained, intrinsically. Thus, no problem is found specially from the layer.

The metallic layer 40 covering the aluminum titanium nitride layer shown in Figs.5 and 6 should preferably be at least one of <sup>which has</sup> noble metals <sup>excellent</sup> (in) anti-oxidizing properties, that is, platinum, iridium, and ruthenium. For the conventional structure in which the anti-oxidizing layer is made of titanium nitride, the metallic layer had to be about 200nm in thickness. For the aluminum titanium nitride layer of the present invention, the resistance to oxidation is already improved. For example, 30nm will do as the thickness of the metallic layer as long as the layer

can cover the surface of the aluminum titanium nitride layer completely.

For the structure shown in Fig. 5, an oxide dielectric layer 16 is formed on the metallic layer 40. However, a conductive oxide layer 60 may be inserted between the oxide dielectric layer 16 and the metallic layer 40 as a component of the lower electrode layer. The conditions for forming a conductive oxide layer in an oxidizing atmosphere are usually the same as those of forming an oxide dielectric layer. Thus, it may be considered that the resistance to oxidization required for the aluminum titanium nitride layer is also the same. Since such a conductive oxide layer can improve the contact property at each interface with a metallic layer, if it includes the same elements of a noble metal as those of the metallic layer, it should preferably be at least one of  $\text{IrO}_2$ ,  $\text{RuO}_2$ ,  $\text{SrRuO}_3$ , and  $\text{ReO}_3$ .  $\text{IrO}_2$ ,  $\text{RuO}_2$ ,  $\text{SrRuO}_3$ , and  $\text{ReO}_3$ .

Hereunder, preferred materials for the oxide dielectric layer 16 will be described. There is no reason to limit the materials for the layer 16 specially. The following materials usable for the layer 16 are well known. Typical examples of oxide dielectrics whose center element is titanium are lead zirconate titanate obtained by replacing part or <sup>all</sup> ~~whole~~ of <sup>the</sup> titanium with zirconium, lead barium zirconate titanate obtained by replacing part or <sup>all</sup> ~~whole~~ of the lead with barium, barium strontium titanate

including only alkaline-earth metal elements, etc. As typical examples of bismuth dielectrics with a layered structure, there are bismuth layered dielectrics such as  $\text{Bi}_4\text{Ti}_3\text{O}_{12}$ ,  $\text{SrBi}_2\text{Ta}_2\text{O}_9$ , etc. In addition to those examples, other well-known oxide dielectrics, oxide ferroelectrics, and new oxide dielectrics and oxide ferroelectrics to be discovered in the future are all usable as the oxide dielectric layer described above.

The upper electrode layer 17 may be any material if it is conductive. <sup>The materials</sup> (They) are not limited only to metals and oxides. Each of the noble metals described above (in the example of the metallic layer 40 provided in the lower electrode layer) is usable. Each of the oxides described above (in the example of the conductive oxide layer 60 provided in the lower electrode layer) is usable. The materials of the upper electrode layer 17 are not limited only to those specially <sup>mentioned</sup>.

Next, description will be made (for) a method (for) manufacturing the semiconductor device of the present invention in order to achieve the second object described above. The method (for) manufacturing the semiconductor device of the present invention includes a process for forming the lower electrode layer including an anti-diffusion and anti-oxidation layer of aluminum titanium nitride which is formed in a nitriding atmosphere using the



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sputtering method. Various types of sputtering targets are usable; for example, a metallic target consisting of a titanium aluminum alloy, a composite-target obtained by putting an aluminum metal or aluminum nitride on a titanium target, a composite-target obtained by putting a titanium metal or a titanium nitride on an aluminum target, a dual target consisting of a titanium target and <sup>an</sup> aluminum target [and so as to be] sputtered simultaneously, a nitride target consisting of an aluminum titanium nitride, a composite-target obtained by putting an aluminum metal or an aluminum nitride on a titanium nitride target, a composite-target obtained by putting a titanium metal or a titanium nitride on an aluminum nitride target, a dual target consisting of an aluminum nitride target and a titanium nitride target separately and so as to be sputtered simultaneously, <sup>may be employed</sup> [etc]. Any of DC and AC can be used for the sputtering discharge. If an aluminum nitride whose resistance is large is used as a target, however, an RF discharging is required.

At least, a discharge gas and a nitrogen gas must be included in the atmosphere used for forming an anti-diffusion and anti-oxidation layer of aluminum titanium nitride. <sup>An</sup> [A] inert gas can be used as a discharge gas. However, usually an argon gas is used <sup>in consideration of</sup> [considering the] economy. A nitrogen gas is included in the discharge gas by 10 to 90 mole%, since it requires sufficient nitridation

and a high through-put (high deposition rate). If there is no restriction for both semiconductor device and environment, a few percent ammonia gas may be included thereby to accelerate nitridation and suppress oxidation.

The temperature should preferably be above <sup>an</sup> (the) room temperature to 600 °C (included) when (a) aluminum titanium nitride anti-diffusion and an anti-oxidation layer are to be formed with the sputtering method. Of course, (the) room temperature does not mean that samples are kept in the room temperature, but it means that the samples should not be cooled or heated specially. Natural rising of the temperature should be allowed during the sputtering. When a sample was formed at a temperature above 600 °C in a heating process, it was observed by an X-ray diffraction measurement that an aluminum nitride (AlN) was generated separately from the sample.

Furthermore, in order to achieve the second object described above, the method <sup>of</sup> ~~for~~ manufacturing the semiconductor device of the present invention includes a process for completing the lower electrode layer by stacking a metal layer, or a metal layer and a conductive oxide layer sequentially on an anti-diffusion and anti-oxidation layer of aluminum titanium nitride. On this lower electrode layer, an oxide dielectric layer is formed. Then, the upper electrode layer is stacked thereon so that an oxide

Before the oxide dielectric capacitor, that is, the lower electrode layer is formed, part of a MOS transistor is formed on the substrate. The lower electrode layer is connected electrically to the source area or the drain area of this MOS transistor through the conductive material filled in the contact holes perforated in the insulator, which covers the semiconductor substrate on which the MOS transistor itself is formed. Polycrystalline silicon formed using the chemical vapor deposition method is often used as the conductive material filled in these contact holes. The forming method and the filling material are not limited specially.

### 3. Characteristics of the Semiconductor Device of the Present Invention

The semiconductor device to be realized by an embodiment of the present invention on the basis of the above two guidelines for selecting conductive materials will have the following characteristics.

The semiconductor device of the present invention is provided with <sup>a</sup>(the) first area (a semiconductor substrate or a semiconductor film, etc.) consisting of a conductive semiconductor material, <sup>a</sup>(the) second area connected to the first area and consisting of the first conductive material, <sup>a</sup>(the) third area connected to the second area and consisting of the second conductive material, <sup>a</sup>(the) fourth area connected to the third area and consisting of an oxide <sup>dielectric</sup>dielectric, and <sup>a</sup>(the) fifth area connected to the fourth area and consisting of a conductive material. And, the average resistivity of the first area is almost equal to the resistivity of the semiconductor material composing the first area and the average resistivity of the second area is almost equal to the resistivity of the first conductive material composing the second area. Such <sup>a</sup>(the) characteristics mean that the respective electric resistances of the first to third areas are determined uniquely by the resistivity of the semiconductor material or the conductive material used for forming each of those areas, as well as by the length of the current path in each of those areas (or the thickness of each of those areas, if

it is stacked vertically). In other words, the embodiment of the present invention can avoid the forming of a high resistant material almost completely in the first <sup>area</sup> or second area, which has been a problem of the conventional technology. And accordingly, it is possible to suppress an increase of the electrical resistance in those areas, as well as enabling the average resistivity in the current path from the first area to the third area to be set <sup>to</sup> 0.01  $\Omega$ cm or below.

Consequently, according to the present invention, when both <sup>the</sup> oxide dielectric layer and <sup>the</sup> conductive oxide layer are formed, memory cells can be formed without oxidizing the polycrystalline silicon layer adjacent to both <sup>the</sup> oxide dielectric layer and <sup>the</sup> conductive oxide layer, as well as the anti-diffusion non-oxide conductive layer consisting of a nitride, etc. Consequently, it becomes possible to reduce both <sup>the</sup> interfacial resistance and <sup>the</sup> contact resistance of each electrode, obtaining a semiconductor device provided with fine-structured memory cells, suitable for high integration. In addition, the semiconductor device of the present invention can omit a process for forming a metallic layer of 200nm or over in thickness consisting of platinum and the like as an anti-oxidizing layer, [as well <sup>and</sup> as] it can reduce the total thickness and the aspect ratio of the capacitor by thinning the lower electrode layer. It is thus

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possible for the present invention to obtain a semiconductor device provided with fined-structured memory cells to be formed through a fine-patterned process of <sup>the</sup><sub>1</sub> submicron region, for example, using (a) gigabit class lithographic technology.

Brief Description of the <sup>Drawing</sup> [Invention]  
*is a diagram which*

Fig. 1 <sub>1</sub> illustrates an oxide dielectric capacitor provided with a double-layered conductive oxide layer included in its lower electrode layer.

*is a diagram which*  
Fig. 2 <sub>1</sub> illustrates an oxide dielectric capacitor provided with a double-layered conductive oxide layer formed on a polycrystalline silicon layer.

*is a diagram which*  
Fig. 3 <sub>1</sub> illustrates an oxide dielectric capacitor provided with a double-layered conductive oxide layer formed on an anti-diffusion non-oxide conductive layer.

*is a diagram which*  
Fig. 4 <sub>1</sub> illustrates an oxide dielectric capacitor provided with a double-layered conductive oxide layer formed on an anti-diffusion non-oxide conductive layer through a metallic layer.

*is a diagram which*  
Fig. 5 <sub>1</sub> illustrates an oxide dielectric capacitor provided with an oxide dielectric layer on a metallic layer stacked on an aluminum titanium nitride layer.

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is a diagram which  
Fig. 6 illustrates an oxide dielectric capacitor

provided with an oxide dielectric layer on a conductive

oxide layer stacked on an aluminum titanium nitride layer.

Fig. 7(a) and 7(b) are graphs which illustrate  
[Fig. 7 illustrates] the electrical characteristics of

the oxide dielectric capacitor formed so as to form a

double-layered conductive oxide on a polycrystalline

silicon layer. Fig. 7(a) illustrates the electrode resistance and Fig. 7(b)

(b) illustrates a polarization hysteresis curve.

Fig. 8(a), 8(b) and 8(c) are graphs which illustrate  
[Fig. 8 illustrates] the electrical characteristics of

the oxide dielectric capacitor formed so as to form a

double-layered conductive oxide on a nitride layer. Fig. 8(a)

illustrates the resistance of an electrode including a TiN  
layer and Fig. 8(b) illustrates the resistance of an electrode

including a TaN layer and Fig. 8(c) illustrates a polarization

hysteresis curve of a capacitor including a TiN layer.

is a graph which  
Fig. 9 illustrates a polarization hysteresis curve of

an oxide dielectric capacitor formed so as to form a

double-layered conductive oxide layer on a TiN layer through

a metallic layer.

Fig. 10(a) and 10(b) are graphs which illustrate  
[Fig. 10 illustrates] a compositional range of an

aluminum titanium nitride. Fig. 10(a) indicates the  
allowance in

( $Ti_{1-x}Al_x$ )<sub>0.5</sub>N<sub>0.5</sub>. Fig. 10(b) indicates the y allowance in ( $Ti_{0.6}Al_{0.4}$ )

1-y N<sub>y</sub>.

is a graph which

Fig. 11 illustrates a polarization hysteresis curve of  
an oxide dielectric capacitor provided with an aluminum

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titanium nitride layer. <sup>Conver</sup> A (a) indicates a case <sup>where</sup> ~~(that)~~ an oxide dielectric layer stacked on a metallic layer and <sup>can't</sup> A (b) indicates a case <sup>where</sup> ~~(that)~~ an oxide dielectric layer is stacked on a conductive oxide layer.

<sup>is a diagram which</sup>  
Fig. 12, illustrates a manufacturing process of the semiconductor device of the present invention (in an embodiment).

<sup>is a diagram which</sup>  
Fig. 13, illustrates a manufacturing process of the semiconductor device of the present invention (in an embodiment).

<sup>is a diagram which</sup>  
Fig. 14, illustrates a manufacturing process of the semiconductor device of the present invention (in an embodiment).

<sup>is a diagram which</sup>  
Fig. 15, illustrates a manufacturing process of the semiconductor device of the present invention up to a planarizing process (in an embodiment).

<sup>is a diagram which</sup>  
Fig. 16, illustrates a manufacturing process of the semiconductor device in which a double-layered conductive oxide layer is formed on a polycrystalline silicon layer.

<sup>is a diagram which</sup>  
Fig. 17, illustrates a manufacturing process of the semiconductor device in which a double-layered conductive oxide layer is formed on an anti-diffusion non-oxide conductive layer.

<sup>is a diagram which</sup>  
Fig. 18, illustrates a manufacturing process of the semiconductor device in which a double-layered conductive

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is a diagram which

is a diagram which

is a diagram which

according to an

provided

## 1-1 Guideline 1 for selecting conductive materials

At first <sup>a</sup>

reference to the accompanying drawings if a double-layered conductive oxide layer is selected for two conductive oxide layers provided between a semiconductor layer and a dielectric layer in an electrode of an oxide dielectric capacitor suitable for a semiconductor device.

<First Embodiment>

In the first embodiment of the present invention, the resistance of the lower electrode layer and the polarization hysteresis curve of an oxide ferroelectric capacitor were measured with respect to the lower electrode layer 11 formed so as to form a conductive oxide layer 14 with oxygen deficiency in a double-layered conductive oxide layer 12 shown in Fig.2 directly on a polycrystalline silicon layer 20.

At first, an amorphous silicon layer doped with phosphorus of 150nm in thickness was formed on a 15mm square conductive silicon substrate 10 by [the] chemical vapor deposition. The substrate was then annealed thereby obtaining a conductive polycrystalline silicon layer 20. Then, two types of samples were formed on this substrate. One sample was formed as follows; at first, conductive oxide layers 14 and 15 were formed through a 2mm square metal mask, then they were further shrunken down to a 100  $\mu$ m square by electron beam lithography. This sample was used for measuring the resistance of the object electrode. The other

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sample was formed as follows; at first, conductive oxide layers 14 and 15 were formed on the entire surface of the substrate, then an oxide dielectric layer 16 and the upper electrode layer 17 were stacked like a pyramid through a 4mm square metal mask and another metal mask of 2mm in diameter, respectively. Then, the upper electrode layer 17 was shrunken down to a  $10\text{ }\mu\text{m}$  square by ion milling using a photo mask. This sample was used for measuring the characteristics of the object capacitor.

To form the conductive oxide layers 14 and 15,  $\text{IrO}_2$ ,  $\text{RuO}_2$ ,  $\text{SrRuO}_3$ ,  $\text{SrTiO}_3$  to which La was added by 4 weight%, and  $\text{ReO}_3$  were used (in this embodiment, chemical formulas are used to clarify each compound. The description of the oxygen deficiency is omitted for convenience [s] sake). Next, how to form each oxide layer will be described. However, the methods described here for manufacturing each compound are just examples. They may be exchanged (by) each other.

The electron beam deposition method was used only for forming  $\text{IrO}_2$ . At first, the  $\text{IrO}_2$  oxide powder was molded into a (cylinder) shape of 12mm in diameter and 10mm in thickness using a pressure die. After this, it was annealed at  $1100\text{ }^\circ\text{C}$  for 2 hours in an oxygen gas flow. This was used as an electron beam source. Then, a  $[\text{IrO}_2]$  layer with oxygen deficiency was formed under the following conditions: temperature of the substrate heater;  $600\text{ }^\circ\text{C}$ , deposition

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rate; 2nm/min. and pressure;  $0.1 \mu\text{Torr}$ . After this, oxygen gas was introduced up to a pressure of  $70 \mu\text{Torr}$ . At the same time, the substrate heater was set to  $580^\circ\text{C}$  thereby stacking a  $50\text{nm IrO}_2$  layer to obtain a double-layered conductive oxide layer 12.

The conductive oxide layers other than  $\text{IrO}_2$  were formed by the RF-magnetron sputtering method using a sintered oxide target consisting of the above cation composition. An oxide dielectric layer of 5 to  $50\text{nm}$  in thickness with oxygen deficiency was formed on the following film deposition conditions: temperature of the substrate heater;  $600^\circ\text{C}$ , incident power;  $1.5\text{W}/\text{cm}^2$ , deposition rate;  $3\text{nm}/\text{min}$ , and discharge Ar gas pressure of  $3\text{N}$  in purity;  $3\text{mTorr}$ . After this, oxygen was introduced at  $\text{Ar}/\text{O}_2=9/1$  and the substrate heater was set to  $580^\circ\text{C}$ , thereby forming a conductive oxide layer so as to form a double-layered conductive oxide layer 12.

The oxide dielectric layer 16 was formed using the RF-magnetron sputtering method using bismuth titanate ( $\text{Bi}_4\text{Ti}_3\text{O}_{12}$ ), which is one of bismuth layered ferroelectrics. The target was a sintered material represented by the above cation composition. The film deposition conditions are as follows: temperature of the substrate heater;  $600^\circ\text{C}$ , discharge gas/oxygen gas pressure ratio;  $\text{Ar}/\text{O}_2=9/1$ , total pressure;  $5\text{mTorr}$ , incident power;  $1.5\text{W}/\text{cm}^2$ , deposition

rate; 5nm/min. and thickness; 200nm. The type and preparation method of the oxide dielectric layer just affected the substantial physical properties of the capacitor. There was recognized no influence on the double-layered conductive oxide layer. On the upper electrode layer <sup>the</sup> ~~it~~ was <sup>deposited</sup> ~~deposited~~ a gold film of 100nm in thickness using the electron beam deposition method.

Fig.7(a) shows the total resistance (vertical axis) of the entire lower electrode layer as a function of the thickness (horizontal axis) of the conductive oxide layer with oxygen deficiency, formed in a non-oxidizing atmosphere. The resistance was measured between the conductive oxide layer formed in an oxidizing atmosphere and the conductive silicon substrate. In any <sup>of the</sup> conductive oxide electrodes, if the oxygen deficient layer was 5nm in thickness, the electrode resistance was very large. Thus, it was clear that polycrystal silicon was oxidized, thereby increasing the resistance. If the oxygen deficient layer was 5 to 10nm in thickness, the resistance dropped sharply and the layer was 10nm or over in thickness, then the resistance was almost constant. From this result, it was clear that the covering ratio of the surface of the polycrystal silicon increased and that the oxidation of the polycrystal silicon was suppressed. It was because of a resistivity difference affected on the conductive oxide

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layer itself that the electrode resistance depended on the type of the oxide electrode.

The <sup>resistivity</sup> [resistivity] of a conductive oxide material itself, when measured for another single layer film, was only a few tens of  $\mu\Omega\text{cm}$  or so for  $\text{IrO}_2$ ,  $\text{RuO}_2$ , and  $\text{RuO}_3$  and as low as two or three times of that even in the oxygen deficient film. As for  $[\text{SrRuO}_3]$ , if oxygen deficiency was introduced, the resistivity increased just within  $200\ \mu\Omega\text{cm}$  to a few  $\text{m}\Omega\text{cm}$ . For  $\text{SrTiO}_3$  to which La was added by 4 weight%, the resistivity increased within a few hundreds of  $\mu\Omega\text{cm}$  to a few  $\text{m}\Omega\text{cm}$ . These results matched with the tendency shown in Fig.7(a) and indicated that the <sup>resistivity</sup> [resistivity] did not increase remarkably even when the double-layered conductive oxide electrode grew adjacent to the polycrystalline silicon.

Fig.7(b) <sup>shows</sup> (show s) a polarization hysteresis curve of an oxide ferroelectric capacitor that uses oxide electrodes when the oxygen deficient layer is 30nm in thickness. There is no difference in the hysteresis curve between the types of oxide electrodes. As shown clearly in Fig.7(b), if a conductive oxide layer adjacent to polycrystalline silicon is formed in a non-oxidizing atmosphere, both oxidation and oxygen diffusion are suppressed. It is thus possible to prove that a voltage supplied from the substrate can be applied effectively to the oxide dielectric layer.

<Second Embodiment>

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In the second embodiment of the present invention, the resistance of the lower electrode layer and the polarization hysteresis curve of the oxide ferroelectric capacitor were measured with respect to the structure of the lower electrode layer 11. In the lower electrode layer 11 provided in the double-layered conductive oxide layer 12 shown in Fig.3, the conductive oxide layer 14 with oxygen deficiency<sub>1</sub> is formed on a conductive nitride layer which functions as an anti-diffusion non-oxide conductive layer 30.

At first, an amorphous silicon film with a thickness of 150nm was formed on the 15mm square conductive silicon substrate 10 using the chemical vapor deposition while doping<sup>with</sup> phosphorus. Then, the amorphous silicon film was annealed thereby to form a conductive polycrystalline silicon layer 20. After this, a conductive nitride layer, which would function as an anti-diffusion non-oxide conductive layer 30, was formed all over the substrate. On this ground layer was formed two types of samples. One sample was formed as follows; conductive oxide layers 14 and 15 were formed through a 2mm square metallic mask, then the layers 14 and 15 were shrunken down to a 100  $\mu\text{m}$  square [respectively] by electron beam lithography. The sample was used for measuring electrode resistance. The other sample was formed as follows; conductive oxide layers 14 and 15 were formed all over the surface of the substrate, then an oxide

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dielectric layer 16 and an upper electrode layer 17 were stacked like a pyramid through a 4mm square metallic mask and a 2mm diameter metallic mask, respectively, and further the upper electrode layer 17 was shrunken down to a  $10\text{ }\mu\text{m}$  square by electron beam lithography. The sample was used for measuring capacitor characteristics.

In this embodiment, TiN and TaN were used as a<sub>1</sub><sup>a</sup> conductive nitride layer (anti-diffusion non-oxide conductive layer 30), which will be described below in detail. The film deposition method and the obtained results were also the same with respect to Zr, Nb, V, and W nitrides. A conductive nitride layer was formed using a<sub>1</sub><sup>a</sup> DC sputtering method (that used <sup>very</sup> a metal target). The film deposition conditions were as follows: temperature of the substrate heater;  $300\text{ }^{\circ}\text{C}$ , discharge gas/nitrogen gas pressure ratio;  $\text{Ar/N}_2 = 50/50$ , total pressure;  $4\text{ mTorr}$ , incident power;  $400\text{W}$ , and film thickness:  $40\text{nm}$ . The RF-magnetron sputtering method can also be used for forming the conductive nitride layer. The method may use a nitride target instead of the metallic target. After the film deposition, an annealing treatment was applied to the sample so as to accelerate crystallization using the rapid thermal annealing method at  $800\text{ }^{\circ}\text{C}$  for two minutes in an ammonia gas atmosphere.



For the <sup>conductive</sup> conductive oxide layers 14 and 15, compounds of  $\text{IrO}_2$ ,  $\text{RuO}_2$ ,  $\text{SrRuO}_3$ ,  $\text{CaRuO}_3$  and  $\text{ReO}_3$  were used respectively. (Chemical formula were just used to clarify each compound here. The description of the amount of oxygen deficiency was omitted for the convenience [s] sake.) Each oxide layer was formed as follows. Each deposition method described here was just an example. The deposition method could also be replaced with another.

The compound  $\text{IrO}_2$  <sup>was</sup> ~~was~~ formed in a weak oxidizing atmosphere using the RF-magnetron sputtering method. The target was a sintered oxide one. The film deposition conditions were as follows: temperature of the substrate heater:  $600^\circ\text{C}$ , incident power:  $1.5\text{W}/\text{cm}^2$ , discharge gas; Ar gas of 3N in purity and 3 mTorr in pressure, and weak oxidizing gas;  $\text{N}_2\text{O}$  gas of  $\text{Ar}/\text{N}_2\text{O}=100/1$  in flow ratio. Under those conditions, a conductive oxide layer with oxygen deficiency was formed with a film thickness of 5 to 50nm. Then, the gas flow ratio was lowered to  $\text{Ar}/\text{N}_2\text{O}=9/1$ , as well as the total pressure was set to 5 mTorr and the temperature of the substrate heater was set to  $580^\circ\text{C}$  to form a 50nm conductive oxide layer, thereby forming a double-layered conductive oxide layer 12.

$\text{SrRuO}_3$  and  $\text{CaRuO}_3$  were formed in an Ar gas atmosphere using <sup>a</sup> ~~(the)~~ RF-magnetron sputtering method that <sup>employs</sup> ~~(used)~~ a sintered oxide target. The film deposition conditions were

as follows: temperature of the substrate heater; 600 °C, incident power; 1.5W/cm<sup>2</sup>, and discharge gas; Ar gas of 3N in purity and 3 mTorr in pressure. Under those conditions, a conductive oxide layer with oxygen deficiency was formed with a film thickness of 5 to 50nm. Then, oxygen was introduced at a gas flow ratio of Ar/O<sub>2</sub>=9/1. (as well as) the total pressure was set to 5 mTorr and the temperature of the substrate heater was set to 580 °C to form a 50nm conductive oxide layer 12.

RuO<sub>2</sub> and <sup>ReO<sub>3</sub></sup>[ReO<sub>3</sub>] were formed in a weak oxidizing atmosphere using the reactive evaporation method. A metal block was used as the evaporation source. The film deposition conditions were as follows: temperature of the substrate heater; 600 °C, deposition rate; 1 nm/min, and oxygen pressure; 5 μTorr. Under those conditions, an oxygen deficient layer was formed with a thickness of 5 to 50nm, then oxygen was introduced at a pressure up to 70 μTorr, (as well as) the temperature of the substrate heater was lowered to 580 °C thereby to stack the 50nm thick RuO<sub>2</sub> and ReO<sub>3</sub> layers, so that a double-layered conductive oxide layer 12 was formed.

For the oxide dielectric <sup>layer</sup> [layer] 16, lead zirconate titanate [ Pb(Zr<sub>0.5</sub>Ti<sub>0.5</sub>)O<sub>3</sub> ] was used. The RF-magnetron sputtering method was used to form the layer 16. The target

was a sintered one represented by the above cationic composition. The film deposition conditions were as follows: temperature of the substrate heater; 600 °C, discharge gas/oxygen gas pressure ratio;  $\text{Ar}/\text{O}_2 = 9/1$ , total pressure; 5 mTorr, incident power;  $1.5 \text{ W}/\text{cm}^2$ , deposition rate; 5 nm/min, and film thickness; 200nm. The type and film deposition method of the oxide dielectric layer affected only the substantial physical characteristics of the capacitor and did not affect the double-layered conductive oxide film. The upper electrode layer 17 was formed with the same conductive oxide as that of the lower electrode layer in an oxidizing atmosphere using the RF-magnetron sputtering method. The film thickness was 80nm.

$\text{TiN} \left[ \begin{smallmatrix} (F_{4.8}(a)) \\ ((a) \text{ in Fig. 8}) \end{smallmatrix} \right]$  and  $\text{TaN} \left[ \begin{smallmatrix} (F_{4.8}(b)) \\ ((b) \text{ in Fig. 8}) \end{smallmatrix} \right]$ , were used respectively for forming the anti-diffusion non-oxide conductive layer 30. The resistance (vertical axis) of the entire lower electrode layer was shown as a function of the thickness (horizontal axis) of the oxygen deficient layer. The resistance was measured between the conductive oxide layer formed in an oxidizing atmosphere and the conductive silicon substrate. The resistance depended on the thickness of the oxygen deficient layer in the same way as the above regardless of the type, deposition method, and deposition conditions of the nitride layer and the conductive oxide electrode. The electrode resistance was significantly ~ high

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when the oxygen deficient layer was 5nm in thickness. This was because the interface was oxidized, thereby the resistance was increased when the coating ratio of the nitride layer surface was small and a conductive oxide layer was formed in the subsequent oxidizing atmosphere. The resistance was reduced sharply as the thickness was between 5nm and 10nm and almost constant at 10nm or over. This was because the coating rate of the nitride layer surface was increased, <sup>and</sup> thereby the oxidization of the phase boundary was suppressed. The reason why the resistance was high when using  $\text{CaRuO}_3$  for an oxide electrode was an increase of the contact resistance at the electrode interface. This was confirmed using the X ray diffraction method. As for an electrode including  $(\text{IrO}_2, \text{RuO}_2, \text{and ReO}_3)$  layers formed in a weak-oxidizing atmosphere, the resistance was slightly larger than that of an electrode including  $\text{SrRuO}_3$  formed in the Ar gas. In any compounds, it was clear that the resistance was kept low enough to be used for the object electrode layer. The resistivity of a conductive oxide material itself was as described in the first embodiment of the present invention when measured for the respective single layer film of  $(\text{IrO}_2, \text{RuO}_2, \text{ReO}_3, \text{SrRuO}_3, \text{and SrTiO}_3)$  obtained by adding La by 4 weight%. The resistivity of the  $\text{CaRuO}_3$  when the film was formed in a non-oxidizing atmosphere, increased up to a little less than several

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hundreds of  $\mu\Omega\text{cm}$  to  $10\text{ m}\Omega\text{cm}$ . These results coincide with the tendency shown in Fig. 8(a), indicating that the resistance did not increase so much even when the double-layered conductive oxide electrodes grew (in) adjacent to the anti-diffusion non-oxide conductive layer 30.

Fig. 8(c) shows a polarization hysteresis curve of an oxide ferroelectric capacitor when the oxygen deficient layer is 10nm in thickness in a case <sup>where</sup> (that) TiN is used as a nitride layer. For an electrode that includes a CaruO<sub>3</sub> layer, the hysteresis curve is opened to the horizontal axis more than those of other electrodes. This seems to be because of the decomposed CaO comes the distribution in the electric field which is applied to dielectrics. However, there is no problem, since characteristics are good enough for the capacitor. As shown in Fig. 8(c) clearly, it is proved that if a conductive oxide layer is formed adjacent to a nitride layer in a non-oxidizing atmosphere, both oxidation and oxygen diffusion are suppressed, thereby a voltage can be applied to the oxide dielectric layer effectively from the substrate. The same hysteresis curve as that shown in Fig. 8(c) was also obtained for the TaN layer.

<Third Embodiment>

In the third embodiment of the present invention, the polarization hysteresis curve for an oxide ferroelectric

capacitor was measured with respect to the structure of the lower electrode layer 11, in which the conductive oxide layer 14 with oxygen deficiency is formed on an anti-diffusion non-oxide conductive layer 30 via metallic layer 40. The layer 14 is provided in the double-layered conductive oxide layer 12 shown in Fig. 4.

The shapes and film deposition methods of the substrate 10, the polycrystalline silicon layer 20, a TiN layer or the anti-diffusion non-oxide conductive layer 30, as well as the oxide dielectric layer 16 and the upper electrode layer 17 are the same as those in the first and second embodiments described above. It is not essential to select the materials of the oxide dielectric layer and the upper electrode layer, however, <sup>in the</sup> in the embodiments of the present invention.

The TiN layer was formed with a thickness of 40nm in accordance with the method of the second embodiment. The TiN layer was used as an anti-diffusion non-oxide conductive layer 30. The same results were also obtained for other nitrides listed in the above second embodiment.

In this embodiment, platinum was used for the metallic layer 40. The same effect was also found when iridium and ruthenium, which are the same nobles metals as platinum, were used. The DC sputtering method was used for forming the metallic layer on the following conditions: Incident

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✓ power; 400W, discharge gas; Ar, gas pressure; 20 mTorr, and temperature of the substrate heater: 500 °C. The metallic layer 40 was thus formed with a thickness of 20nm on the whole area of anti-diffusion non-oxide conductive layer 30.

$\text{IrO}_2$ ,  $\text{RuO}_2$ ,  $\text{SrRuO}_3$ , and  $\text{SrTiO}_3$  to which La was added by 4 weight% were used for forming the conductive oxide layer using (the) RF-magnetron sputtering method in a weak oxidizing atmosphere. The targets were <sup>made of</sup> a sintered oxide (one) [respectively]. The film deposition conditions were as follows: temperature of the substrate heater; 600 °C, incident power;  $1.5 \text{ W/cm}^2$  discharge gas; Ar gas of 3N in purity and 3 mTorr in pressure, and weak oxidizing gas;  $\text{N}_2\text{O}$  gas of  $\text{Ar}/\text{N}_2\text{O}=100/1$  in flow ratio. Under these conditions, the conductive oxide layer 14 with oxygen deficient layer of 10nm in thickness was formed. Then, the gas flow ratio was lowered to  $\text{Ar}/\text{N}_2\text{O}=9/1$ , as well as the total pressure was set to 5 mTorr and the substrate heater was set to 580 °C to form a 50nm thick conductive oxide layer 15, thereby forming a double-layered conductive oxide layer 12.

Fig. 9 shows a polarization hysteresis curve of an oxide ferroelectric capacitor with respect to each conductor oxide. Regardless of the oxygen deficient layer type, the hysteresis curve was an <sup>open</sup> (opened) one with high symmetry. Even when the metallic layer was as thin as 20nm and a conductor oxide layer adjacent to this metallic layer

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was formed in a weak oxidizing atmosphere, the oxygen deficient layer included in the conductive oxide layer was found to be effective for suppressing oxidation and oxygen diffusion, thereby a voltage could be applied effectively to the oxide dielectric layer from the substrate.

As described above in each of the <sup>embodiments</sup> [embodiments] of the present invention, a conductive oxide layer with oxygen deficiency was formed in a non-oxidizing atmosphere, which is one of the characteristics of the present invention, thereby forming a double-layered conductive oxide layer. Consequently, the lower electrode layer and the oxide dielectric layer could be formed without oxidizing the polycrystalline silicon (the first embodiment of the present invention) adjacent to the double-layered conductive oxide layer, the anti-diffusion non-oxide conductive layer consisting of (an) nitrides, etc. adjacent to the double-layered conductive oxide layer, as well as the anti-diffusion non-oxide conductive layer (the second embodiment of the present invention) adjacent to the double-layered conductive oxide layer through a metallic layer. Consequently, it was possible to reduce the interfacial resistance and contact resistance of each electrode, thereby forming an oxide dielectric capacitor suitable for high integration.



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Hereunder, <sup>a</sup> description will be made <sup>to indicate</sup> [for] how to select an aluminum titanium nitride layer at the side of the semiconductor and an anti-oxidization metallic layer at the side of the dielectrics of the two conductive material layers provided between a semiconductor layer and a dielectric layer in the electrode of an oxide dielectric capacitor suitable for a semiconductor device. The accompanying drawings will be referenced for describing the fourth and fifth embodiments of the present invention.

<Fourth Embodiment>

In the fourth embodiment of the present invention, the allowable contents of both aluminum and nitrogen were checked in an aluminum titanium layer with respect to the phase uniformity, low resistivity, and resistance to oxidation. The phase uniformity and the resistance to oxidation were checked by the X ray diffraction method and the resistivity was measured using the DC four-point (probe) <sup>probe</sup> method.

At first, an aluminum titanium nitride  $[(Ti_{1-x}Al_x)_{1-y}N_y]$  film was formed on a conductive silicon substrate using the DC sputtering method. A natural oxidized film was already removed from the substrate before this deposition. The target was a composite one obtained by spreading aluminum and titanium metallic plates in a mosaic fashion all over an aluminum metal plate. The aluminum content  $x$  was adjusted

according to the area ratio of both metallic plates. The nitrogen content  $y$  was adjusted by changing the argon discharge gas/nitrogen gas flow ratio within the range of 95/5 to 5/95. The substrate heater was set to 550 °C. Other film deposition conditions were as follows: Incident power; 400W, total gas pressure; 5 to 20 mTorr, growth rate; 5 to 10 nm/min, and film thickness; 50nm. The aluminum content  $x$  was analyzed and determined using the ICPS method (Inductively-Coupled Plasma Spectroscopy) and the nitrogen content  $y$  was analyzed and determined using the RBS (Rutherford Back Scattering) method that uses  $\text{He}^+$  ions.

Fig.10(a) shows both reaction products and <sup>the</sup> resistivity of a sample whose nitrogen content  $y$  is 0.5 as a function of the aluminum content  $x$ . As a result of X ray diffraction, only a diffraction line assignable to TiN was observed when  $x$  was 0.6 or below. If  $x$  exceeded 0.6, however, a mixed phase with a phase assignable to AlN was observed. As the  $x$  value increased, the TiN phase disappeared and the AlN phase increased. The resistivity increased a little as the  $x$  value increased. The resistivity increased sharply around 0.5. Fig.10(b) shows both reaction products and resistivity of a sample whose aluminum content  $X$  is 0.4 as a function of the nitrogen content  $y$ . As a result of X ray diffraction, diffraction lines other than TiN were observed if the  $y$  value was smaller than 0.2 or exceeded 0.6. The

resistivity was checked only for the nitrogen content whose y value was 0.2 to 0.6 (included). For this nitrogen content, a single phase was observed in the X ray diffraction pattern. The resistivity increased as the y value increased. And, the resistivity increased sharply around 0.6 of the y value. Usually, an effect of the impurity phase is observed in the resistivity more than in X ray diffraction. Thus, the threshold values of both x and y to be determined by a resistivity seems to be narrowed.

Next, a platinum layer with a thickness of 30nm was formed by the DC sputtering method on the aluminum titanium layer formed above. The film deposition conditions were as follows: Incident power; 400W, discharge gas; Argon gas, gas pressure; 20 mTorr, and deposition temperature; 500 °C. On the platinum layer was stacked an oxide dielectric layer [Pb(Zr<sub>0.5</sub>Ti<sub>0.5</sub>)O<sub>3</sub>] with a thickness of 100nm, using RF-magnetron sputtering. The film deposition conditions were as follows: temperature of the substrate heater; 300 °C, incident power; 1.5W/cm<sup>2</sup>, deposition rate; 3 nm/min, discharge Ar gas/oxygen gas flow ratio; 90/10, and pressure; 5 mTorr. After the 100nm thick oxide dielectric layer was formed, rapid thermal annealing was applied to the layer at 650 °C for 2 minutes in an oxygen flow, thereby to accelerate the crystallization of the layer.

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Finally, the oxide dielectric layer, after it was formed once, was removed completely in a dry etching process, thereby exposing the platinum layer again. An X ray diffraction measurement was made for this sample to check if the aluminum titanium nitride  $[(Ti_{1-x}Al_x)_{1-y}N_y]$  layer was oxidized and changed in quality by the formed oxide dielectric layer. Fig. 10<sup>(c)</sup> also shows this result. As shown in Fig. 10(a), it was confirmed that the oxide layer was oxidized, thereby  $TiO_2$  was formed when the aluminum content  $x$  was smaller than 0.2. And, as shown in Fig. 10(b),  $TiO_2$  was also observed when the nitrogen content  $y$  was smaller than 0.4.

The above threshold values remained the same even when both aluminum and nitrogen contents  $x$  and  $y$  were fixed at another value respectively.

The above threshold values also remained the same substantially even when platinum was replaced with any of iridium, ruthenium, and rhenium for forming the metallic layer. And, the aluminum titanium nitride layer for preventing oxygen diffusion and oxidation was also effective to other oxide dielectrics, for example, lead zirconate titanate having a different titanium/zirconium ratio, lead barium zirconate titanate, barium strontium titanate, and bismuth ferroelectrics.

<Fifth Embodiment>

In the fifth embodiment of the present invention, the polarization hysteresis curve of an oxide dielectric capacitor including an aluminum titanium nitride layer for preventing oxygen diffusion and oxidation was measured. <sup>(Fig. 11)</sup>

For the sample (a), an oxide dielectric layer was stacked directly on the platinum layer of 30nm in thickness/aluminum titanium nitride layer of 50nm in thickness/conductive silicon substrate described in the fourth embodiment of the present invention. For the sample (b), an oxide dielectric layer was stacked on the above layer through a conductive oxide layer.

A  $\text{RuO}_2$  layer of 50nm in thickness was formed as the conductive oxide layer using the RF-magnetron sputtering method. The target was an Ru metal one. The film deposition conditions were as follows: temperature of the substrate heater; 500 °C, incident power; 1.5W/cm<sup>2</sup>, deposition rate; 3 nm/min, discharge Ar gas/oxygen gas flow ratio; 50/50, and pressure; 7 mTorr.

Lead zirconate titanate [  $\text{Pb}(\text{Zr}_{0.5}\text{Ti}_{0.5})\text{O}_3$  ] layer of 100nm in thickness was formed as the oxide dielectric layer using the sol-gel method. Sol was a solution obtained by making lead acetate, titanium isopropoxide and zirconium isopropoxide react <sup>with</sup> (to) each other in methoxy ethanol. This solution was coated on the platinum layer [sample (a)] or on the conductive oxide layer [sample (b)], then rapid ~

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thermal annealing was applied to each sample at 650 °C for two minutes in an oxidizing atmosphere, thereby crystallizing the sample.

A 2mm diameter platinum layer was formed as the upper electrode layer through a metallic mask using the DC sputtering method.

Fig. 11 shows a polarization hysteresis curve (appeared) (and) measured when a voltage was applied [to] between the upper electrode layer and the conductive silicon substrate. For both samples (a) and (b), good hysteresis curves were obtained. Even when the platinum layer put therebetween was as thin as 30nm, the aluminum titanium nitride layer functioned effectively to prevent oxygen diffusion and oxidation. It was thus confirmed that the object capacitor operation was satisfactory with a voltage supplied from the substrate.

To select <sup>certain</sup> (the) materials of a conductive oxide layer and an oxide dielectric layer is not essential in the embodiments of the present invention. For example, any of the conductive oxides of  $\text{IrO}_2$ ,  $\text{SrRuO}_3$ , and  $\text{ReO}_3$  can be used to obtain the same effect. In addition, any of lead zirconate titanate  $[\text{Pb}(\text{Zr}_x\text{Ti}_{1-x})\text{O}_3]$  with  $x$  other 0.5, strontium barium titanate  $[(\text{Ba}_x\text{Sr}_{1-x})\text{TiO}_3(x=0 \text{ to } 1)]$ , lead barium zirconate titanate, and bismuth layered

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ferroelectrics can be used to form the object capacitor in the same way.

As described in each of the embodiments of the present invention, if an aluminum titanium nitride layer for preventing oxygen diffusion and oxidation, which is one of the characteristics of the present invention, was formed, then the lower electrode layer and the oxide dielectric layer could be formed without oxidizing the nitride layer even when adjacent metallic layers including the platinum one were thinned down to 30nm. Consequently, the interfacial resistance and the contact resistance of each electrode, as well as the capacitor aspect ratio could be reduced, thereby forming an oxide dielectric capacitor suitable for high integration.

## 2. How to Form a Semiconductor Device Provided with a Dielectric Capacitor

Next, description will be made for how an oxide dielectric capacitor of the present invention is used in a semiconductor device. A MOS transistor formed on a silicon substrate will be picked up as an example for the description with reference to the accompanying drawings with respect to the sixth to tenth embodiments of the present invention to be described below. The sixth to eight and ninth to tenth embodiments are based on the guideline 1 and 2 for selecting conductive materials respectively as described above.

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<Sixth Embodiment>

In this sixth embodiment of the present invention, description will be made at first for the pre-process up to the forming of an oxide dielectric capacitor with respect to the manufacturing method of a semiconductor device.

At first, description will be made for how to form a MOS transistor on a silicon substrate, then how to planarize the surface of the substrate once and finally for how to form a polycrystalline silicon plug used to connect the capacitor electrode electrically to the MOS transistor. The series of manufacturing processes will be described sequentially with reference to Figs. 12 to 15.

As shown in Fig. 12, a <sup>switching</sup> transistor is formed in an existing MOSFET integrating process. 121 <sup>denotes</sup> is a p-type semiconductor substrate, 122 <sup>denotes</sup> is an isolating insulator between devices, 123 <sup>denotes</sup> is a gate oxide film, 124 <sup>denotes</sup> is a word line used as a gate electrode, and 125 and 126 <sup>denotes</sup> are n-type impurity diffusion layers in which phosphorus is doped respectively. 127 <sup>denotes</sup> is a passivation layer consisting of <sup>SiO<sub>2</sub></sup> <sup>Reference numeral</sup> 128. Next, the surface is covered completely with a 50nm thick SiO<sub>2</sub> layer 128 by the chemical vapor deposition. After this, the surface is covered once with a 600nm thick Si<sub>3</sub>N<sub>4</sub> layer 129, then this Si<sub>3</sub>N<sub>4</sub> layer 129 is etched as deep as the deposited film thickness, thereby filling the insulator between word lines. The structure is thus formed as shown in Fig. 12. The

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SiO<sub>2</sub> layer 128 is an under layer for producing the bit lines in a subsequent process and <sup>is</sup> used to prevent <sup>exposing of the</sup> surface of the substrate, as well as <sup>damage to the</sup> (damaged) isolating insulator 122 between elements.

Fig.13 shows the next process. The Si<sub>3</sub>N<sub>4</sub> portion where a bit line to be formed later will come in contact with the n-type impurity diffusion layer 125 on the surface of the substrate, as well as the Si<sub>3</sub>N<sub>4</sub> portion where a capacitor electrode to be formed later will come in contact with the n-type impurity diffusion layer 126 on the surface of the substrate are processed respectively so as to be perforated with holes using <sup>a</sup>(the) photo-lithography method and <sup>a</sup>(the) dry etching method. After this, amorphous silicon including <sup>an</sup> n-type impurity is deposited with a thickness of 600nm all over the portion including the holes, <sup>and is</sup> then annealed so as to be crystallized. The polycrystalline silicon is then etched as deep as the film thickness, so as to be structured as shown in Fig.13. Consequently, the holes are filled with polycrystalline silicon 131 and 132.

Fig.14 shows the next process for forming a bit line. At first, the entire surface is covered with the SiO <sup>2</sup> SiO<sub>2</sub> insulator 141 using the chemical vapor deposition. Then, the <sup>SiO<sub>2</sub></sup> SiO <sup>2</sup> insulator positioned above the polycrystalline silicon 131 is perforated with holes using both photo-lithography method and dry etching method so that the bit

line to be formed later are connected to the n-type impurity diffusion layer 125 electrically. After this, metallic silicide to become a bit line later, as well as a polycrystalline silicon layer (142) are formed all over these holes. And, on the layer 142 is deposited an  $\text{SiO}_2$  layer 143 with a thickness of 200nm. The  $\text{SiO}_2$  layer 143, the metallic silicide, and the polycrystalline silicon layer 142 are then patterned using both photo-lithography and dry-etching methods, thereby forming a bit line 142 and an  $\text{SiO}_2$  layer 143. Then, to insulate the side wall of the bit line 142,  $\text{Si}_3\text{N}_4$  is deposited with a thickness of 150nm using the chemical vapor deposition, then etched using the dry-etching method, thereby forming an  $\text{Si}_3\text{N}_4$  side wall spacer 144. Finally, the  $\text{SiO}_2$  insulator 141 positioned above the polycrystalline silicon 132 is treated using both photo-lithography and dry-etching methods, thereby making holes. These holes are used to connect a capacitor electrode to be formed later to the n-type impurity diffusion layer 126 electrically.

Fig. 15 shows the process for planarizing the surface of the substrate and forming a conductive polycrystalline silicon plug before the object capacitor is formed. At first, an insulator 151 is deposited on the substrate with a thickness <sup>sufficient</sup> (enough) to planarize the surface of the substrate. In this embodiment of the present invention, a

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500nm thick boron phosphorus silicate glass (BPSG) is used, but another silicon oxide film may be used instead of the BPSG. The glass is planarized by chemical mechanical polishing. The surface of the substrate can also be covered by  $\text{SiO}_2$  using the chemical vapor deposition, then etched back to planarize the surface. Next, the photo-lithography and the dry etching method are applied to the insulator 151 positioned above the n-type impurity diffusion layer 126, thereby making contact holes. After this, phosphorus-doped amorphous silicon is deposited all over the surface including <sup>these</sup> ~~(these)~~ holes with a thickness of 200nm using the chemical vapor deposition, <sup>and</sup> ~~then~~ <sup>this</sup> annealed to crystallize the surface. The surface is then etched back using the dry etching method, thereby forming each polycrystalline silicon plug 152 filled with polycrystalline silicon.

This completes the pre-process for forming the oxide dielectric capacitor.

Next, description will be made for respective processes for forming an oxide dielectric capacitor including a double-layered conductive oxide later on the substrate for which a MOS transistor and a polycrystalline silicon plug are already formed. In this embodiment, the lower electrode takes a structure in which a conductive oxide layer with oxygen deficiency is formed directly on the polycrystalline silicon shown in Fig. 2.

At first, as shown in Fig.16, a 10nm thick conductive oxide layer 161 ( $\text{RuO}_2$ ) with oxygen deficiency is formed in an Ar atmosphere using the RF-magnetron sputtering method as described in detail in the first embodiment of the present invention. Then, oxygen is introduced at a gas flow ratio up to  $\text{Ar}/\text{O}_2=9/1$ , (as well as) the total pressure is increased, thereby stacking a 50nm thick conductive oxide layer 162 so as to form a double-layered conductive oxide layer (161 and 162). After this, the layer (161 and 612) was covered with a 50nm thick W film using the DC sputtering method. Then, a photo resist masking pattern was transferred onto the surface of the layer (161 and 162) using the dry etching method. This transferred pattern was used as a mask to pattern the double-layered conductive oxide layer (161 and 162) using the sputtering etching method. Then, the transferred mask was removed by etching and an oxide dielectric layer 163 was formed. In the embodiments of the present invention, lead zirconate titanate [ $\text{Pb}(\text{Zr}_{0.5}\text{Ti}_{0.5})\text{O}_3$ ] was used as <sup>an</sup>oxide, <sup>dielectric</sup>(dielectrics). The deposition method was as described in detail in the second and third embodiments of the present invention. The film thickness was 100nm. Finally, a platinum cell plate electrode 164 was formed to complete the object memory cell capacitor.

The polarization hysteresis characteristics of the oxide ferroelectric capacitor (sample) were measured by

changing the capacitor area from 0.2 to 25  $\mu\text{m}^2$ . As a result, a satisfactory hysteresis curve was obtained, enabling a voltage to be supplied to the oxide dielectric layer from the polycrystalline silicon plug 152 in any cases.

In the embodiments of the present invention, it is not essential (whether) to select <sup>a particular material for the</sup> an oxide dielectric layer. Any of lead zirconate titanate  $[\text{Pb}(\text{Zr}_x\text{Ti}_{1-x})\text{O}_3]$  with y other than 0.5, strontium barium titanate  $[(\text{Ba}_x\text{Sr}_{1-x})\text{TiO}_3 (x=0 \text{ to } 1)]$ , lead barium zirconate titanate, and bismuth layered ferroelectrics can be used to form memory cells in the same way. In addition, the same effect could be obtained for the conductive oxide layer using any of the compounds described in the first embodiment of the present invention.

<Seventh Embodiment>

In this seventh embodiment of the present invention, description will be made (for) <sup>of</sup> a process for forming an oxide dielectric capacitor on a substrate after finishing the processes from forming a MOS transistor up to forming a polycrystalline silicon plug as described in detail in the sixth embodiment of the present invention. The capacitor includes a double-layered conductive oxide layer formed on an anti-diffusion non-oxide conductive layer as shown in Fig. 3.

At first, as shown in Fig. 17, an anti-diffusion oxide conductive layer 171 is formed. In this embodiment,  $\text{TiN}$  is

used for the anti-diffusion non-oxide conductive layer and such an example will be described in detail. However, note that the same effect was also obtained for the semiconductor device of the present invention when any of the nitrides of Ta, Zr, Nb, V, and W <sup>were</sup> ~~was~~ used. The nitride layer, as described in detail in the second embodiment of the present invention, was formed using the DC sputtering method that <sup>employed</sup> ~~A~~ <sup>A</sup> (used) a metallic target. The film thickness was 40nm. After the film deposition, the sample was annealed at 800 °C for two minutes in an ammonia gas atmosphere using the rapid thermal annealing method, thereby accelerating the crystallization of the film.

Next, an  $\text{SrRuO}_3$  layer was formed in a weak oxidizing atmosphere using the RF-magnetron sputtering method. The layer was used as a double-layered conductive oxide layer. The same effect can be obtained even with the film deposition in an Ar gas atmosphere. Then, a conductive oxide layer 161 ( $\text{SrRuO}_3$ ) with a 10nm thick oxygen deficient layer was formed at a gas flow ratio of  $\text{Ar}/\text{O}_2=100/1$ . <sup>and</sup> ~~A~~ then the gas flow ratio was lowered to  $\text{Ar}/\text{O}_2=9/1$  thereby stacking a 50nm conductive oxide layer 162 so as to form the double-layered conductive oxide layer (161 and 162). The film deposition conditions including the temperature were the same as those in the second embodiment of the present invention described above.

Next, the above layers were covered with a 50nm W film and a photo-resist masking pattern was transferred to the W film using the dry etching method. This transferred pattern was used as a mask for patterning the double-layered conductive oxide layer (161 and 162), as well as the anti-diffusion non-oxidizing conductive layer 171 through sputter-etching. The transferred mask was then removed and an oxide dielectric layer 163 was formed. In the embodiments of the present invention, lead zirconate titanate  $[\text{Pb}(\text{Zr}_{0.5}\text{Ti}_{0.5})\text{O}_3]$  was used as <sup>an</sup> oxide <sup>dielectric</sup> ~~dielectrics~~. The film deposition method was the same as ~~those~~ described in the second and third embodiments of the present invention in detail. The film thickness was 100nm. Finally, a platinum electrode 164 was formed to complete the object capacitor of a memory cell.

The sample was then measured with respect to the polarization hysteresis characteristics of this oxide ferroelectric capacitor by changing the capacitor area from 0.2 to 25  $\mu\text{m}^2$ . As a result, it was found in <sup>all</sup> ~~any~~ cases that a voltage could be supplied from the polycrystal silicon plug 152 to the oxide dielectric layer so as to obtain a satisfactory hysteresis curve.

In the embodiments of the present invention, it is not essential ~~(whether)~~ <sup>a particular material for the</sup> to select ~~(an)~~ oxide dielectric layer. Any of lead zirconate titanate  $[\text{Pb}(\text{Zr}_x\text{Ti}_{1-x})\text{O}_3]$  with x other than

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0.5, strontium barium titanate  $[(Ba_x Sr_{1-x})TiO_3 (x=0 \text{ to } 1)]$ , lead barium zirconate titanate, and bismuth layered ferroelectrics can be used to form memory cells. The same effect could also be obtained using any of the compounds,  $IrO_2$ ,  $RuO_2$ ,  $CaRuO_3$ ,  $SrTiO_3$  to which La is added, and  $ReO_3$  for the conductive oxide layer as described in the first to this embodiments of the present invention.

#### <Eighth Embodiment>

In this eighth embodiment of the present invention, description will be made  $(f_{ox})^1$  a process for forming an oxide dielectric capacitor on a substrate after finishing the processes from forming of a MOS transistor up to forming of a polycrystalline silicon plug as described in detail in the sixth embodiment of the present invention. The capacitor includes a double-layered conductive oxide layer formed on an anti-diffusion non-oxide conductive layer through a metallic layer as shown in Fig. 4.

At first, as shown in Fig. 18, an anti-diffusion oxide conductive layer 171 is formed. In this embodiment, TiN is used for the anti-diffusion non-oxide conductive layer and such an example will be described below. However, note that the same effect was also obtained for the semiconductor device of the present invention when any of the nitrides of Ta, Zr, Nb, V, and W was used. The TiN layer was formed as described in detail in the seventh embodiment of the present



invention. On this layer <sup>was formed</sup> [was further formed] a 20nm thick metallic layer 181, using the DC sputtering method. Although platinum was used in this embodiment, it was confirmed that the same effect was also obtained with the use of iridium and ruthenium. The film deposition conditions for the metallic layer were the same as those in the third embodiment of the present invention.

Next, an  $(\text{IrO}_2)$  layer was formed in a weak oxidizing atmosphere using the RF-magnetron sputtering method. The layer was used as a double-layered conductive oxide layer. Of course, the same effect was obtained even with the film deposition in an Ar gas atmosphere. Then, a 10nm conductive oxide layer 161 ( $\text{IrO}_2$ ) with oxygen deficiency was formed at a gas flow ratio of  $\text{Ar}/\text{O}_2=100/1$ , then the gas flow ratio was lowered to  $\text{Ar}/\text{O}_2=9/1$  so as to stack a 50nm conductive oxide layer 162  $(\text{IrO}_2)$ , thereby forming a double-layered conductive oxide layer (161 and 162). The film deposition conditions including the temperature were the same as those in the third embodiment of the present invention described above.

Next, the above layer was covered with a 50nm W film and a photo-resist masking pattern was transferred to the W film using the dry etching method. [As this] <sup>this</sup> transferred pattern mask was used for patterning the double-layered conductive oxide layers 161 and 162 and metallic layer 181.

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as well as <sup>for</sup> the anti-diffusion non-oxidizing conductive layer 171 through sputter-etching. The transferred mask was then removed and an oxide dielectric layer 163 was formed. In the embodiments of the present invention, lead zirconate titanate [  $\text{Pb}(\text{Zr}_{0.5}\text{Ti}_{0.5})\text{O}_3$  ] was used as <sup>an</sup> oxide <sup>dielectric</sup> ~~dielectrics~~. The film deposition method was the same as those described in the second and third embodiments of the present invention in detail. The film thickness was 100nm. Finally, a platinum cell plate electrode 164 was formed to complete the object capacitor of a memory cell.

The sample was then measured with respect to the polarization hysteresis characteristics of this oxide ferroelectric capacitor by changing the capacitor area from 0.2 to 25  $\mu\text{m}^2$ . As a result, it was found in <sup>all</sup> ~~(any)~~ cases that a voltage could be supplied from the polycrystal silicon plug 152 to the oxide dielectric layer so as to obtain a satisfactory hysteresis curve.

In the embodiments of the present invention, it is not essential <sup>a particular material for the</sup> ~~(whether)~~ to select <sup>(an)</sup> oxide dielectric layer. Any of lead zirconate titanate [  $\text{Pb}(\text{Zr}_x\text{Ti}_{1-x})\text{O}_3$  ] with X other than 0.5, strontium barium titanate [  $(\text{Ba}_x\text{Sr}_{1-x})\text{TiO}_3$  ] ( $x=0$  to 1), lead barium zirconate titanate, and bismuth layered ferroelectrics can be used to form memory cells in the same way. The same effect could also be obtained using any of the compounds,  $\text{RuO}_2$ ,  $\text{SrRuO}_3$ ,  $\text{CaRuO}_3$ ,  $\text{SrTiO}_3$  to which  $\text{La}$  is

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added, and  $\text{ReO}_3$  as described in the first to third embodiments of the present invention for the conductive oxide layer.

<Ninth Embodiment>

In this ninth embodiment of the present invention, description will be made <sup>of</sup> (For) a process for forming an oxide dielectric capacitor on a substrate after finishing the processes from forming of a MOS transistor up to forming of a polycrystalline silicon plug as described in detail in the sixth embodiment of the present invention. The capacitor includes an aluminum titanium nitride layer for preventing oxygen diffusion and oxidation. In this embodiment, the lower electrode layer takes a structure in which a metallic layer and an oxide dielectric layer are stacked sequentially on the aluminum titanium nitride shown in Fig. 5.

At first, as shown in Fig. 19, an aluminum titanium nitride  $[(\text{Ti}_{0.7}\text{Al}_{0.3})_{0.5}\text{N}_{0.5}]$  layer 191 was formed using the RF-magnetron sputtering method. The target was a composite one obtained by <sup>depositing</sup> (putting) a proper amount of aluminum nitride plate on a titanium nitride plate. The film deposition conditions were as follows: temperature of the substrate heater; 550 °C, incident power; 400W, total gas pressure; 8 mTorr, argon discharge gas/nitrogen gas flow ratio; 90/10, deposition rate; 10 nm/min, and film thickness; 50nm. The

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same effect to be described below was also obtained using another aluminum or nitrogen content, <sup>as indicated</sup> described in Fig. 5.

On this layer <sup>was formed</sup> [was further formed] a 30nm thick metallic layer 181 using the DC sputtering method. Although platinum was used in this embodiment, it was confirmed that the same effect was also obtained with the use of iridium and ruthenium. The film deposition conditions for the metallic layer were the same as those in the fourth embodiment of the present invention.

Next, the layer formed above was covered with a 50nm W film and a photo-resist masking pattern was transferred to the W film using the dry etching method. Using this transferred pattern as a mask, the aluminum titanium nitride layer 191 and the metallic layer 182 were patterned through sputter-etching. The transferred mask was then removed and an oxide dielectric layer 163 was formed. In the embodiments of the present invention, lead <sup>zirconate titanate</sup> [Pb(Zr<sub>0.5</sub>Ti<sub>0.5</sub>)O<sub>3</sub>] was used as <sup>an</sup> <sup>dielectric</sup> oxide, <sup>dielectrics</sup>. The film deposition method was the sol-gel method as described in the fifth embodiment of the present invention in detail. The film thickness was 100nm. Finally, a platinum electrode 164 was formed and patterned to complete the object capacitor of a memory cell.

The sample was then <sup>measured</sup> [measure] d with respect to the polarization hysteresis characteristics of this oxide

ferroelectric capacitor by changing the capacitor area from 0.2 to 25  $\mu\text{m}^2$ . As a result, it was found in <sup>all</sup> (any) cases that a voltage could be supplied from the polycrystal silicon plug 152 so as to obtain a satisfactory hysteresis curve.

In the embodiments of the present invention, it is not essential (whether) <sup>a particular material as the</sup> to select (any) oxide dielectric layer. Any of lead zirconate titanate  $[\text{Pb}(\text{Zr}_x\text{Ti}_{1-x})\text{O}_3]$  with x other than 0.5, strontium barium titanate  $[(\text{Ba}_x\text{Sr}_{1-x})\text{TiO}_3(x=0 \text{ to } 1)]$ , lead barium zirconate titanate, and bismuth layered ferroelectrics can be used to form memory cells in the same way.

<Tenth Embodiment>

In this tenth embodiment of the present invention, description will be made (to) <sup>of</sup> a process for forming an oxide dielectric capacitor on a substrate after finishing the processes from forming of a MOS transistor up to forming of a polycrystalline silicon plug as described in detail in the sixth embodiment of the present invention. The capacitor includes an aluminum titanium nitride layer for preventing oxygen diffusion and oxidation. In this embodiment, the lower electrode layer takes a structure in which a metallic layer, a conductive oxide layer, and an oxide dielectric layer were stacked sequentially on the aluminum titanium nitride shown in Fig. 5.

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At first, as shown in Fig. 20, an aluminum titanium nitride  $[(Ti_{0.5}Al_{0.5})_{0.5}N_{0.5}]$  layer 191 and a metallic layer 181 were formed using the same method as that in the ninth embodiment. The same effect to be described below was also obtained using another aluminum or nitrogen content, as well as using iridium, ruthenium, and rhenium.

A 50nm thick  $IrO_2$  layer formed using the RF-magnetron sputtering method was used as the conductive oxide layer 201. The target was an Ir metal one. The film deposition conditions were as follows: temperature of the substrate heater; 500 °C, incident power; 1.5W/cm<sup>2</sup>, deposition rate; 3 nm/min, discharge Ar gas/oxygen gas flow ratio; 50/50, and pressure; 7 mTorr.

Next, the layer formed above was covered with a 50nm W film and a photo-resist masking pattern was transferred to the W film using the dry etching method. Using this transferred pattern as a mask, the aluminum titanium nitride layer 191, the metallic layer 181, as well as a conductive oxide layer 201 were patterned through sputter-etching.

The transferred mask was then removed and an oxide dielectric layer 163 was formed. In the embodiments of the present invention, bismuth layered ferroelectrics,  $Bi_4Ti_3O_{12}$ , was used as <sup>the</sup>oxide / <sup>dielectric</sup>dielectrics. In an oxidizing atmosphere at 50  $\mu$ Torr in pressure, the titanium and bismuth were evaporated using an electron gun and an effusion cell

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respectively, thereby forming a 100nm thick amorphous oxide layer [in the] room temperature. After this, a rapid thermal annealing treatment was applied to the sample at 700 °C for 2min in an oxygen atmosphere so as to crystallize the surface. Finally, a platinum cell plate electrode 164 was formed and patterned to complete the object capacitor of a memory cell.

The sample was then measured with respect to the polarization hysteresis characteristics of this oxide ferroelectric capacitor by changing the capacitor area from 0.2 to 25  $\mu\text{m}^2$ . As a result, it was found in (any) cases that a voltage could be supplied from the polycrystal silicon plug 152 to the oxide dielectric layer so as to obtain a satisfactory hysteresis curve.

Whether to select a conductive oxide layer or an oxide dielectric layer is not essential in the embodiments of the present invention. In addition, any of lead zirconate titanate [ $\text{Pb}(\text{Zr}_x\text{Ti}_{1-x})\text{O}_3$ ]( $x=0$  to 1), strontium barium titanate [ $(\text{Ba}_x\text{Sr}_{1-x})\text{TiO}_3$ ]( $x=0$  to 1), lead barium zirconate titanate, bismuth layered ferroelectrics, and  $\text{SrBi}_2\text{Ta}_2\text{O}_9$  can be used to form the object capacitor in the same way. Any of the conductive oxides of  $\text{RuO}_2$ ,  $\text{SrRuO}_3$ ,  $\text{ReO}_3$  can also be used to obtain the same effect.

As described in each of the embodiments of the present invention, a MOS transistor formed on a silicon substrate

is applied to a semiconductor device provided in an oxide dielectric capacitor of the present invention. As for the guideline 1 for selecting conductive materials, a conductive oxide layer with oxygen deficiency was formed in a non-oxidizing atmosphere, thereby forming a double-layered conductive oxide layer. Consequently, the object memory cell was formed without oxidizing the polycrystalline silicon (the sixth embodiment of the present invention) adjacent to the double-layered conductive oxide layer, the anti-diffusion non-oxide conductive layer consisting of a nitride, etc. (the seventh embodiment of the present invention), and the anti-diffusion non-oxide conductive layer (the eighth embodiment of the present invention) through a metallic layer. In accordance with the guideline 2 for selecting conductive materials, an aluminum titanium nitride layer for preventing oxygen diffusion and oxidation was formed, thereby stacking an oxide dielectric layer (the ninth embodiment of the present invention) and a conductive oxide layer (the tenth embodiment of the present invention) without oxidizing the nitride layer even when the metallic layer consisting of platinum, etc. and adjacent to the aluminum titanium nitride layer for preventing oxygen diffusion and oxidation was thinned down to 30nm. The object memory cell could be formed <sup>such</sup> <sup>a</sup> way. According to the

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structures and film deposition methods described above, it became possible to reduce both interfacial resistance and contact resistance of the object electrode, as well as to reduce the capacitor aspect ratio. It was thus possible for the present invention to obtain a semiconductor device provided with fine-structured memory cells suitable for high integration.

In the above embodiments of the present invention, the semiconductor of the present invention was mainly applied to a MOSFET. The semiconductor can also be applied to other devices that use oxide dielectrics (including oxide ferroelectrics) as a capacitor, for example, a GaAs MMIC that uses oxide dielectrics as a so-called path condensor and a chip condensor.

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## SPECIFICATION

Title of the Invention

SEMICONDUCTOR DEVICE AND ITS MANUFACTURING METHOD

## Technical Field

The present invention relates to a semiconductor device suitable for LSIs, as well as a method for manufacturing such a semiconductor. The semiconductor device uses oxide dielectrics, especially oxide ferroelectrics as its capacitor.

## Background Art

Semiconductor devices consisting of LSIs such as dynamic random access memories ( DRAMs), etc. have been confronted with problems that the capacitor area must be reduced to cope with high integration of the object LSI, as well as such a semiconductor device must be prevented from complicated structure caused by the reduction of such the capacity area. In order to solve those problems, therefore, it has been examined to use oxide dielectrics and oxide ferroelectrics as the insulator of the capacitor instead of the silicon oxide and the silicon nitride having been used so far. The relative dielectric constants of both oxide

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dielectrics and oxide ferroelectrics are as large as several hundreds to several thousands. (The oxide dielectrics mentioned here do not include silicon oxides, etc. It means so-called dielectrics whose relative dielectric constants are several hundreds.) The ferroelectrics has spontaneous polarization and its polarity can be reversed using an external electric field. The reversed polarity can also be held. It has thus been tried to use such the ferroelectrics for non-volatile memories. A conventional memory composed of such ferroelectrics is disclosed in the official gazette of Unexamined Published Japanese Patent Application No. Sho-63-201998 (since oxide ferroelectrics can be regarded to be dielectrics at temperatures above the Curie temperature, hereunder, a word of dielectrics will be used to describe the ferroelectrics representatively).

Generally, lead zirconate titanate, strontium barium titanate, and the like are used as oxide dielectrics for memories. However, it has been difficult to use oxide dielectric capacitors for semiconductor devices used as conventional memories, etc., since high temperatures above 500 °C are needed to crystallize the oxide dielectrics in an oxidizing atmosphere.

For example, it might be considered to adopt a structure (conventional structure 1; oxide dielectrics/platinum/silicon) so that platinum can be used

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for lower electrode resistant against both oxidation and thermal budget, provided under an oxide dielectric capacitor. However, platinum and silicon react to each other, thereby platinum silicide is formed at their interface. Consequently, the electrical resistance of each electrode increases. Thus, the (conventional structure 1) allowing such a platinum electrode to come directly in contact with both silicon substrate and polycrystalline silicon will not be suitable. Instead of such the conventional structure 1, therefore, another structure was proposed in 1989 IEEE Int. Solid-State Circuits Conf. Digest pp.242-243. In the structure, oxide dielectric capacitors are formed on passivation layer. On the other hand, a MOS transistor is formed outside the capacitor area. And, a conductive wiring layer using aluminum, and the like is applied to connect the source or drain of the MOS transistor to the capacitor. In the case of this method that uses this conductive wiring layer, it is difficult to reduce the area of each memory cell, so the method is not suitable for a memory to be highly integrated.

The official gazette of Unexamined Published Japanese Patent Application No.Hei-3-256358 disclosed a method for highly integrating a memory formed as follows; a semiconductor substrate provided with a MOS transistor formed thereon is coated with an insulating material; on the

substrate an oxide dielectric capacitor is formed. In the method, contact holes are formed in the insulator and a conductive material is filled in the contact holes thereby to connect either of the source or the drain of the MOS transistor electrically to one of the two electrodes of the capacitor. Generally, polycrystalline silicon is used as the conductive material to be filled in the contact holes. This structure, however, could not avoid occurrence of the above problems. In other words, such a structure that crystallizes oxide dielectrics directly on polycrystalline silicon (conventional structure 2; oxide dielectrics/polycrystalline silicon) oxidizes the interface between those materials, thereby forming a reaction insulating layer there. On the other hand, in order to prevent such the formed reaction insulating layer, the (conventional structure 3; oxide dielectrics/platinum/polycrystalline silicon) is required. In this structure, platinum is inserted between polycrystalline silicon and oxide dielectrics to cope with the problem. This structure is substantially the same as the (conventional structure 1) in configuration. Platinum and polycrystalline silicon react to each other, thereby forming silicide. As a result, the electrical resistance of each electrode increases, as well as silicon diffuses into platinum, causing a silicon oxide film to be formed on

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the surface of the platinum and the characteristics of the dielectric capacitor to be deteriorated. Another problem that the elements composing the dielectrics diffuse into the silicon substrate, will occur.

In order to solve those problems, the official gazettes of Unexamined Published Japanese Patent Application No. Hei-4-14862 and No. Hei-4-181766 disclosed the (fourth structure 4; oxide dielectrics/platinum/( Ti, Ta, TiN, etc.)/polycrystalline silicon) having a non-oxide anti-diffusion conductive layer for (formed with Ti, Ta, TiN, etc.) so as to prevent inter diffusion between platinum electrode and silicon.

In addition to platinum, Ti, Ta, TiN, etc. used for electrode components, conductive oxides are also used as each electrode of an oxide dielectric capacitor. Such an example is reported in (Journal of Material Research, Vol. 8 (1993), pp.12). This typical example is the (fifth structure; oxide dielectrics/ruthenium oxide/SiO<sub>2</sub>). If oxide dielectrics can be put directly in contact with ruthenium oxide, an advantage will be obtained; the mechanical adhesive strength at the interface between oxide dielectrics and electrode increases more than when oxide dielectrics is put in contact with a completely different type metallic electrode. Such an increase of the mechanical adhesive strength between oxide dielectrics and electrode

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can improve the characteristics of the oxide dielectric capacitor such as polarization cycle, etc. In this example, the capacitor is formed on  $\text{SiO}_2$ . If the capacitor is formed on polycrystalline silicon, however, ruthenium oxide, which is an oxide, should not be put in contact directly with polycrystalline silicon for the same reasons as in the case of the (conventional structure 1) and the (conventional structure 3). And, in order to prevent such a direct contact, a noble metallic layer made of platinum, ruthenium, and the like should be formed between them. In this case, the (conventional structure 6; oxide dielectrics/ruthenium oxide/(platinum/ruthenium, etc.)/polycrystalline silicon) will be used suitably.

#### Disclosure of the Invention

In the above related art, description was made for the conventional technology to be applied to memories to be integrated more highly by coating a MOS-transistor-formed-semiconductor substrate with an insulating material, then forming an oxide dielectric capacitor thereon. As described above, the source or drain of the MOS transistor is connected electrically to one of the two electrodes of the capacitor through contact holes, which are generally filled with a conductive material consisting of polycrystalline silicon. And, the following two structures

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are adopted for the conventional technology described above:

(Conventional Structure 4)

Oxide dielectrics/platinum/( Ti, Ta, TiN, etc.)/polycrystalline silicon

(Conventional Structure 6)

Oxide dielectrics/ruthenium oxide/(platinum, ruthenium, etc.)/polycrystalline silicon

Each of the above structures includes the following problems.

At first, the (conventional structure 4) will be described. In order to crystallize oxide dielectrics, an oxidizing atmosphere at 500 °C or over is required. Under such a condition, however, oxygen diffuses along grain boundaries, etc. of platinum crystal grains, thereby oxygen reaches the anti-diffusion non-oxide conductive layer (Ti, Ta, TiN, etc.) to oxidize even the layer. Consequently, the electrical resistance of the electrode itself increases. In order to avoid such a problem, the thickness of the platinum layer is increased. This method, however, makes it difficult to process the platinum layer, and result in an increase of a leak current from the side wall of the capacitor. Because, the aspect ratio of the capacitor increases if the memory is highly integrated and the fine capacitor is formed. And, this is why the (conventional

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structure 4) cannot solve the conventional technology problems if Ti, Ta, TiN, etc. are used for an anti-interdiffusion layer.

Next, the (conventional structure 6) will be described. Also in this case, the ruthenium oxide layer is usually formed in an oxidizing atmosphere. Oxygen diffusion reaches up to polycrystalline silicon through the (platinum, ruthenium, etc.) layers, disabling the (conventional structure 6) to solve the conventional technology problems including the one that an insulating layer is formed by an oxidation.

Such the conventional technology problems also occur not only from the materials shown above concretely, but also from layers consisting (platinum, ruthenium, etc.) classified into noble metals, layers consisting of (Ti, Ta, TiN, etc.) classified into an anti-diffusion non-oxide conductive layer, and an ruthenium oxide layer classified into a conductive oxide even when those materials are classified according to more general categories. In other words, both (conventional structure 4) and (conventional structure 6) are represented using more general material categories, that is, oxide dielectric/noble metal/anti-diffusion non-oxide dielectric layer/polycrystalline silicon in the (conventional structure 7) and oxide dielectric/conductor oxide/noble metal/polycrystalline

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silicon in the (conventional structure 8). The problems caused by each of the above layers composing the above capacitor are summarized as follows.

At first, a noble metal layer will arise the following problems. (a) A noble metal layer will possibly cause a high resistance silicide to be formed if it comes in contact with silicon. (b) A noble metal layer will possibly become a diffusion path between chemical elements composing silicon, oxygen, and oxide. The problems arisen from oxide dielectric and conductive oxide layers will be as follows. (c) Such a layer will possibly oxidize electrodes, thereby increasing electrode resistance or insulating electrodes. Finally, an anti-diffusion non-oxide conductive layer will arise the following problem. (d) The layer will possibly be oxidized and its resistance will increase significantly.

If the characteristics of both (conventional structure 7) and (conventional structure 8) are noticed here, the (conventional structure 9) will be reasoned on the analogy of them. The (conventional structure 9) is obtained by compounding both of the structures simply.

(Conventional Structure 9; oxide dielectric/conductive oxide/noble metal/anti-diffusion non-oxide conductive layer/polycrystalline silicon)

In this case, if an anti-diffusion non-oxide conductive layer is inserted, it is possible to solve one

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of the problems (a)(silicidation) and (b)(the diffusion of chemical elements composing silicon and oxides). However, the above problems (b), (c), and (d) related to oxygen diffusion and oxidation of electrodes remain unsolved just like the (conventional structure 4), since the conventional indispensable conditions for forming oxides in an oxidizing atmosphere are not improved yet at all.

In other words, the conventional technology cannot solve the problems such as oxygen diffusion and oxidation both caused by such oxides as oxide dielectrics and conductive oxides against such non-oxides as noble metals, anti-diffusion non-oxide conductive layers and polycrystalline silicon, not only when an oxide comes in contact with polycrystalline silicon directly, but also when an oxide comes in contact with polycrystalline silicon via a noble metal, as well as when an oxide comes in contact with an anti-diffusion non-oxide conductive layer via a noble metal.

As described above, in order to connect an oxide dielectric material to polycrystalline silicon electrically, an anti-oxidation layer must be formed between them. Conventionally, there have been no effective anti-oxidation layer. Instead of such a layer, therefore, a metallic layer consisting of platinum, etc. is formed between them. Unfortunately, oxygen diffuses even at grain

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boundaries of such a metallic layer, thereby reaching the anti-oxidation layer and probably resulting in oxidation of the layer. The thickness of the metallic layer was increased in some cases to compensate the disadvantage, but this resulted in an increase of the aspect ratio of the capacitor. This method will thus be improper for forming fine-structured memory cells. To solve this problem, therefore, a new and effective anti-diffusion or anti-oxidation layer has been awaited.

Under such the circumstances, it is the first object of the present invention to provide a semiconductor device, which can solve the above conventional technology problems. In order to achieve the first object, the semiconductor device of the present invention is provided with a fine-structured memory, which can be highly integrated using an oxide dielectric material (including ferroelectrics) for the insulator of the capacitor.

It is the second object of the present invention to provide a method for manufacturing such a semiconductor device.

In order to solve the above problems, the semiconductor device of the present invention, which includes a capacitor consisting of an oxide dielectric material, connects a semiconductor layer formed on the top surface of a semiconductor substrate or on a substrate to

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an oxide dielectric material via at least two layer areas, each of which consists of a conductive material different from the other. The materials of these two conductor areas (or material compositions) are combined thereby suppressing an increase of the electric resistance generated in the conventional technology in the anti-diffusion or anti-oxidation layer disposed between a semiconductor area and an oxide dielectric material area.

The semiconductor device of the present invention comprises the first area consisting of a semiconductor material which is conductive (wiring layers and electrodes consisting of a semiconductor substrate or a semiconductor film); the second area connected to the first area and consisting of the first conductive material; the third area connected to the second area and consisting of the second conductive material; the fourth area connected to the third area and consisting of an oxide dielectric material; and the fifth area connected to the fourth area and consisting of a conductive material. Thus, the semiconductor device of the present invention has characteristics as follows in terms of the basic configuration; the material composition at the interface adjacent to the second area in the first area is approximately equal to the average material composition of the first area, and the material composition at the interface adjacent to the first area in the second

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area, as well as the material composition at the interface adjacent to the third area in the second area are approximately equal to the average material composition of the second area, respectively. As understood from these characteristics, the third and fifth areas compose a capacitor via the fourth area. The oxide dielectric material composing the fourth area may be replaced with a so-called ferroelectric material indicating a characteristic ( hysteresis) that a polarization value is changed differently between increasing and decreasing an applied electrical field.

The present invention is characterized mainly as follows: The semiconductor is composed so that the first area has a material composition, which is approximately equal to the composition of the semiconductor material composing the first area at the interface adjacent to the second area, and so that the second area has a material composition, which is approximately equal to the composition of the first conductive material at the interface adjacent to the first area and to the third area. In other words, the semiconductor device of the present invention is composed so as to make the material composition approximately homogeneous within the first and second area, respectively. And, there is no material (silicon oxide, metallic silicide, titanium oxide, etc. described above)

that increases the electrical resistance in those areas. The materials that increase the electrical resistance as described above or the materials having an electrical insulating property actually (hereunder, to be referred to as a high resistance material) are formed around each interface between areas in a process in which the second to fourth areas are multi-stacked sequentially on the first area. On the contrary, according to the semiconductor device of the present invention, the first and second conductive materials are selected properly so as to prevent formed high-resistance material at the interface between the first and second areas, as well as at the interface between the second and third areas and further, the first area is formed so that its material composition at the interface adjacent to the second areas becomes approximately equal to the average material composition in the first area, and the second area is formed so that its material composition at the interface adjacent to the first area, as well as at the interface adjacent to the third area become approximately equal to the average material composition in the second area. It will thus be understood clearly here that no high resistance materials are formed at the interface between the third and fourth areas because of the use of a noble metal of the (conventional structure 7) or the use of a conductive oxide of the (conventional

structure 8) in the third area. In addition, an area (layer) consisting of a conductive material composed differently from the first and second conductive materials may be formed between the third and fourth areas thereby to improve the electrical conductivity needed between the first and third areas or improve the conditions for forming the oxide in the fourth area. In terms of the same aspect, an area (layer) consisting of a conductive material composed differently from the first and second conductive materials may be formed between the first and second areas. In short, what is important is that the second and third areas are connected to each other.

In an embodiment of the present invention, it is most important that the first and second conductive materials should be selected properly. There are two guidelines for selecting conductive materials. The object of the first guideline is as follows; two conductive materials are conductive oxides composed of the same chemical element and of the same framework of the crystal structure. The composition ratio of oxygen in the first conductive material is set lower than that in the second conductive material. In other words, the first conductive material is driven into the oxygen deficiency. The object of the second guideline is as follows; aluminum titanium nitride (  $\text{TiAlN}$  ) is used as the first conductive

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material and an anti-oxidation metallic material is used as the second conductive material. In any of the guidelines, the two conductive materials should preferably be selected from those of which resistivity is  $10 \text{ m}\Omega\text{cm}$  ( $0.01 \Omega\text{cm}$ ) or under respectively. Hereunder, the present invention will be described in detail with reference to each of the guidelines. In the following description, the first to third areas (including a conductive material layer if it is provided between the third and fourth areas) will be referred to as the lower electrode and the fifth area as the upper electrode.

1. Guideline 1 for selecting conductive materials

This guideline is decided to form the second and third areas used as a double-layered conductive oxide layer, which can suppress oxygen diffusion and oxidation (the third object of the present invention) in order to achieve the first object of the present invention, as well as to provide a method for manufacturing the double-layered conductive oxide layer, which can suppress oxygen diffusion and oxidation (the fourth object of the present invention) to achieve the second object of the present invention.

Here, description will be made first for the structure of a semiconductor device that uses a capacitor consisting of an oxide dielectric material, especially the structure of a semiconductor device composed of a double-layered

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conductive oxide layer, etc. including a conductive oxide layer with oxygen deficiency. Next, description will be made sequentially for the characteristics and concrete examples of metallic layers, the characteristics and concrete examples of anti-diffusion non-oxide conductive layers, and concrete examples of oxide dielectric materials. Description will also be made for the characteristics and concrete examples of double-layered conductive oxide layers including a conductive oxide layer with oxygen deficiency respectively together with means for achieving the second object of the present invention described above, that is, a method for manufacturing a semiconductor device of the present invention. The method for achieving the third object of the present invention will also be described in detail, together with the method for achieving the first and second objects. The method for achieving the fourth object of the present invention will be described in detail, together with the method for achieving the second object.

Next, description will be made for a semiconductor device that will achieve the first object of the present invention described above. The semiconductor device of the present invention includes a capacitor composed of oxide dielectrics used as an insulator. Fig.1 shows a schematic diagram of such a capacitor composed of oxide dielectrics.

Fig.1 does not show a detailed structure of the capacitor of the semiconductor device, which is composed of oxide dielectrics. It shows multi-stacked layers of the capacitor in order to simplify the structure. An oxide dielectric capacitor consists of a lower electrode layer 11 formed on a substrate (shown only in the direction of the substrate side 10 in Fig.1), an oxide dielectric layer 16 formed on the layer 11, and an upper electrode layer 17 formed on the layer 16. The lower electrode layer 11 includes a conductive oxide layer 12 and this conductive oxide layer 12 consists of two adjacent layers 14 and 15, which have the same crystal structure and consist of the same chemical elements. Each of the layers 14 and 15 has a composition ratio of oxygen different from the other. In other words, only the conductive oxide layer 14 positioned at the substrate side includes oxygen deficiency. These conductive oxide layers 14 and 15 correspond to the second and third areas described above.

In such a semiconductor device, the lower electrode layer 11 is connected electrically to the source area or the drain area of a MOS transistor formed on the substrate via the lower electrode layer component 13 including at least more than one layer formed closer to the substrate than the conductive oxide layer 14 with oxygen deficiency. Hereunder, an example of this lower electrode layer

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component 13 will be described in detail with reference to Figs. 2, 3 and 4.

Fig. 2 shows a configuration of an oxide dielectric capacitor when the lower electrode layer component 13 which is positioned closer to the substrate than the conductive oxide layer 14 with oxygen deficiency in Fig. 1. consists of a conductive polycrystalline silicon layer 20. The conductive polycrystalline silicon layer 20 mentioned here corresponds to the first area described above. A structure in which an oxide comes in contact with silicon directly is not favorable as described above with respect to the conventional structure, since silicon is oxidized unavoidably under typically necessary conditions for crystallizing the oxide, that is, at 500 °C or over in an oxidizing atmosphere. According to the present invention, however, the conductive oxide layer 14 with oxygen deficiency is formed as an adjacent layer of the polycrystalline silicon layer 20, so that the structure as shown in Fig. 2 is realized. The characteristics of the double-layered conductive oxide layer 12 including the conductive oxide layer 14 with oxygen deficiency will be described later.

Fig. 3 shows a configuration of an oxide dielectric capacitor when the component 13 composing the lower electrode layer consists of a non-oxide conductive layer for

anti-diffusion 30 and a conductive polycrystalline silicon layer 20. The lower electrode layer is positioned closer to the substrate side than the conductive oxide material 14 with oxygen deficiency as shown in Fig.1. The anti-diffusion non-oxide conductive layer 30 corresponds to a layer formed between the first and second areas described above. The conventional technologies cannot avoid oxidization of the anti-diffusion non-oxide conductive layer caused by the oxygen that diffuses at grain boundaries in a noble metal at 500 °C or over in an oxidizing atmosphere, even when a noble metal is used to separate the oxide from the anti-diffusion non-oxide conductive layer as seen in the (conventional structure 7). Those are typical conditions needed to crystallize an oxide. Thus, such a structure as allowing an oxide to be put in contact directly with the anti-diffusion non-oxide conductive layer 30 as described above is not suitable. According to the present invention, however, a conductive oxide layer 14 with oxygen deficiency is adjacent to the anti-diffusion non-oxide conductive layer 30, the structure as shown in Fig.3 is thus realized. The characteristics of the double-layered conductive oxide layer 12 including the conductive oxide layer 14 with oxygen deficiency will be described later.

Fig.4 shows a configuration of an oxide dielectric capacitor when the component 13 composing the lower

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electrode layer positioned closer to the substrate side than the conductive oxide material 14 with oxygen deficiency shown in Fig.1 consists of a metallic layer 40, an anti-diffusion non-oxide conductive layer 30, and a conductive polycrystalline silicon layer 20. The metallic layer 40 and the anti-diffusion non-oxide conductive layer 30 correspond to a layer formed between the first and second areas described above respectively. The conventional technologies cannot avoid oxidization of the anti-diffusion non-oxide conductive layer, which caused by the oxygen diffusion through the metallic layer 40 at 500 °C or over in an oxidizing atmosphere, which are typical conditions needed to crystallize oxides. In order to suppress such the oxidization, therefore, the thickness of the metallic layer 40 must be increased as described above. According to the present invention, however, a conductive oxide layer 14 with oxygen deficiency is adjacent to the metallic layer 40. The structure as shown in Fig.4 is thus realized regardless however thin the metallic layer 40 is. The characteristics of the double-layered conductive oxide layer 12 including the conductive oxide layer 14 with oxygen deficiency will be described later.

A noble metal highly resistant to oxidization will be considered as a candidate for forming such the metallic layer. Concretely, among noble metals, at least one of the

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following noble metal elements will be suitable; platinum which is highly resistant to oxidization, ruthenium, or iridium composed of the same element as the noble metal element included in the conductive oxide layer to be described later.

Hereunder, materials suitable for the anti-diffusion non-oxide conductive layer will be described. Necessary conditions to satisfy the requirements of the anti-diffusion non-oxide conductive layer 30 are conductivity at first, then resistance to oxidization, and resistance to reaction with silicon. Compounds to be considered as candidates for the anti-diffusion non-oxide conductive layer 30 are nitride, silicide, boride, and carbide. The anti-reaction to silicon is stable in any of those compounds. Any of them can be used with no problem. Of course, if the object semiconductor device is annealed at 1000 °C or over, the elements of any of those compounds will react to silicon, thereby forming reaction products of high resistance or insulation properties possibly. However, a back-end process including forming of an oxide dielectric capacitor for a semiconductor device will require only a heating condition of 800 °C at highest for a few minutes, which will not form such reaction products caused by mutual diffusion of elements. The reaction to silicon can thus be neglected. As for the resistance to oxidization, there

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will arise no problem in the case of that the conductive oxide layer with oxygen deficiency of the double-layered conductive oxide layer is put adjacent to the anti-diffusion non-oxide conductive layer (Fig.3). As to be described later, this is because the conductive oxide layer with oxygen deficiency must be formed in a non-oxidizing atmosphere and the conductive oxide layer with oxygen deficiency functions as an obstacle in the oxygen diffusion path. In addition, since the conductive oxide layer with oxygen deficiency is over-stacked on the anti-diffusion non-oxide conductive layer 30 with a metallic layer therebetween (Fig.4), the anti-diffusion non-oxide conductive layer 30 is separated farther from the oxide layer. In addition, forming a metallic layer adjacent to the anti-diffusion non-oxide conductive layer have never arisen any problem conventionally.

Hereunder, a concrete example of the anti-diffusion non-oxide conductive layer will be described. A nitride will be suitable if it includes at least one of such metal types Ti, Ta, Zr, Nb, V, and W, since it becomes very conductive. In addition those materials, silicide such as Ti, boride such as La, carbide such as Ti, will also be suitable.

Next, materials suitable for an oxide dielectric layer will be described. Ferroelectric materials are also

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oxide dielectric materials, of course. There is no reason that must limit the materials. There are some well-known materials as shown below, however. Typical examples of oxide dielectrics of which center element is titanium are; lead zirconate titanate obtained by replacing part or whole of the titanium with zirconium, lead barium zirconate titanate obtained by replacing part or whole of the lead with barium, barium strontium titanate including only alkaline earthmetals, etc. As typical examples of bismuth-system dielectrics composed in a layered structure, there are bismuth layered dielectrics such as  $\text{Bi}_4\text{Ti}_3\text{O}_{12}$ ,  $\text{SrBi}_2\text{Ta}_2\text{O}_9$ , etc.

In addition to those well-known oxide dielectrics and oxide ferroelectrics, as well as new oxide dielectrics and oxide ferroelectrics to be discovered in the future, etc. are usable as the oxide dielectric layer described above.

Next, the characteristics of the double-layered conductive oxide layer 12 including a conductive oxide layer with oxygen deficiency will be described, since mentioned so in the description of the structures shown in Figs. 2 to 4. Here, description will be made for the structure, function, and manufacturing method of the double-layered conductive oxide layer in order to achieve the method for manufacturing the semiconductor device, which is the second object of the present invention, the function of the

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As described above, it is oxidizing of the anti-diffusion non-oxide conductive layer and polycrystalline silicon that are already stacked to become a problem when in forming an oxide layer for dielectrics and electrodes. The oxidation is caused by an oxidizing atmosphere, which is indispensable for forming oxide layers. What must be emphasized here that a problem is not reaction between oxide and silicon or between oxide and an anti-diffusion non-oxide conductive layer. In terms of the standard Gibbs free energy, oxides composed of alkali earthmetals such as Sr and Ca, and transition elements such as Ru and Ti are more stable than oxidation of Si. An anti-diffusion non-oxide conductive layer composed of nitride, silicide, boride, and carbide of transition metals cannot be expected to be oxidized through reaction to an oxide in terms of the free energy. If anything, they are all oxidized by an oxidizing active gas in the atmosphere needed for forming an oxide layer. Consequently, the present inventor has concluded that the above problems can be solved if an oxide layer is formed in a non-oxidizing atmosphere in expectation that

other elements composing the semiconductor device of the present invention would not be oxidized.

Generally, the oxide dielectrics (including ferroelectrics) forming an oxide dielectric capacitor and oxide films such as conductive oxide electrodes are formed in an oxidizing atmosphere. This is mainly because oxides are unstable chemically in a non-oxidizing atmosphere and no oxide film is formed or even when it is formed, its characteristics are not satisfactory. Because the vapor pressure of typical elements is high, film formation under an insufficient oxidizing condition surely causes selective evaporation, that is, a variation in composition in oxide ferroelectrics including group-4 and group-5 typical elements such as lead and bismuth. At the same time, since decomposed products other than object compounds also come to be mixed, the ferroelectric properties are degraded significantly. In addition, the non-oxidizing atmosphere causes oxygen deficiency in the object compound. In the case of oxide dielectrics including group-4 transition elements such as titanium and zirconium, oxygen deficiency will cause the dielectric constant to be lowered, as well as causes a leakage current. Consequently, it is not realistic to form an oxide dielectric film in a non-oxidizing atmosphere.

As for another oxide for forming oxide dielectric capacitors, that is, conductive oxide electrodes, it was

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expected that films could be formed in a non-oxidizing atmosphere as long as it does not affect the characteristics of electrodes or the object semiconductor device even when oxygen deficiency was introduced into compounds and simultaneously decomposed products were mixed while the films were formed in a non-oxidizing atmosphere. In other words, the oxygen deficiency reduces or increases the charge density, as well as changes its mobility, thereby increasing its resistivity. However, no problem arises as long as the resistivity required for the electrode layer is secured. Forming of films in a non-oxidizing atmosphere will also arise no problem as long as the resistance required for the electrode layer is secured even when the resistivity is increased by coexistence of some decomposed products.

The component 13 of the lower electrode layer adjacent to the conductive oxide layer 12 in Fig.1, corresponds to the polycrystalline silicon layer 20 in Fig.2, the anti-diffusion non-oxide conductive layer 30 in Fig.3, and the anti-diffusion non-oxide conductive layer 30 through the metallic layer 40 in Fig.4, respectively. In order to prevent those layers from oxidation, the present inventor thought it would be better to form the side 14 at which the conductive oxide layer 12 was adjacent to the component 13 (20, 30 and 40) of the lower electrode layer in a non-oxidizing atmosphere. The layer 14 was thus formed up to

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a certain thickness. And, the rest layer 15 of the conductive oxide layer 12 was formed continuously in an oxidizing atmosphere by changing the oxidizing activity of only the film deposition conditions, such as the oxygen pressure and the type of the oxidizing gas. In other words, the conductive oxide layer 12 is composed of adjacent two layers 14 and 15, and these two layers are composed in the same crystal structure and with the same element, but differently from each other in the composition ratio of oxygen. Only the layer 14 of the two adjacent layers includes oxygen deficiency. The layer 14 is positioned at the composed component 13 side of the lower electrode layer, that is, at the substrate side.

Since the conductive oxide layer 14 is formed in a non-oxidizing atmosphere, the adjacent lower electrode layer component 13 (polycrystalline silicon layer 20, the anti-diffusion non-oxide conductive layer 30, and the metallic layer 40) are not oxidized. The conductive oxide layer 14 with oxygen deficiency, after it is formed once, is stable in terms of the standard Gibbs free energy. Then, the component 13 (20, 30, and 40) of the lower electrode layer is also not oxidized. And, as shown in Fig.4, even when a metallic layer 40 is inserted therebetween, the anti-diffusion non-oxide conductive layer 30 is never be

oxidized by oxygen diffusion, so the thickness can be thinned as much as possible.

After the forming of the conductive oxide layer 14 with oxygen deficiency, the conductive oxide layer 15 and the oxide dielectric layer 16 are formed in an oxidizing atmosphere. If the conductive oxide layer 14 includes oxygen deficiency, the layer 14 acts as a diffusion buffer layer against oxygen even when those layers 15 and 16 are formed in an oxidizing atmosphere. In other words, even when the surface of the conductive oxide layer 14 with oxygen deficiency is exposed to an oxidizing gas, the layer 14 acts as a buffer layer against the oxygen diffusion ions, as well as captures diffusing oxygen ions. Since the conductive oxide layer 14 itself is stable in terms of the standard Gibbs free energy, the layer 14 acts as an anti-oxidation layer for the component 13 (20, 30, and 40) of the lower electrode layer.

Consequently, the double-layered conductive oxide layer including a conductive oxide layer with oxygen deficiency, which is formed in a non-oxidizing atmosphere, acts as an excellent oxidation resistant film and an oxygen diffusion barrier layer.

The thickness of the conductive oxide layer 14 (with oxygen deficiency), which is formed in a non-oxidizing atmosphere, should preferably be 10nm or larger. The reason

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is that the component 13 (20, 30, and 40) of the lower electrode layer is completely covered so as to be prevented from oxidizing when the conductive oxide layer 15 and the oxide dielectric layer 16 are formed in an oxidizing atmosphere. The upper limit is not determined specially for the thickness. All of the conductive oxide layers 12 may be composed of a conductive oxide layer 14 (with oxygen deficiency) which is formed in a non-oxidizing atmosphere. In this case, however, since the following oxide dielectric layer 16 is formed off course in an oxidizing atmosphere, the interface of conductive oxide layer 14 adjacent to the oxide dielectric layer 16 is oxidized. Consequently, a thin layer 15 is formed at the interface. The double-layered conductive oxide layer 12 can thus be formed.

Hereunder, a non-oxidizing atmosphere will be described with respect to a method for manufacturing the double-layered conductive oxide layer. A certain non-oxidizing atmosphere is an atmosphere including a hydrogen gas and a reducing gas. In such a reducing atmosphere, however, much oxygen is takeout while an oxide film is grown in the film deposition process. The film is thus possibly reduced to a metall. A milder non-oxidizing atmosphere is an inactive gas atmosphere that uses inert gasses such as argon and helium, or a vacuum into which none of oxidizing gases such as oxygen ( $O_2$ ), nitride monoxide ( $N_2O$ ), nitric

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dioxide ( $\text{NO}_2$ ), ozone ( $\text{O}_2$ ), etc. is introduced intentionally. If the component 13 of the lower electrode layer is assumed to be an anti-diffusion non-oxide conductive layer 30 (or a metallic layer 40) and a conductive oxide layer to be formed is more reactive to oxygen than the anti-diffusion non-oxide conductive layer 30, it can apply a weak oxidizing atmosphere including oxidizing gases such as oxygen, nitrogen monoxide, nitrogen dioxide and ozone, etc. slightly. In other words, as described in the conventional technologies, it is more possible that the anti-diffusion non-oxide conductive layer is oxidized in a remarkable oxidizing atmosphere. In the atmosphere including a slight oxidizing gas, the anti-diffusion non-oxide conductive layer is not oxidized while a conductive oxide layer with oxygen deficiency can be formed. This is because an energy barrier for oxidation exists between the anti-diffusion non-oxide conductive layer in which compounds are already formed and the conductive oxide layer.

Concretely, the condition of a non-oxidizing atmosphere depends on respective film deposition methods with which a conductive oxide layer is formed. At first, when an oxide film is formed in an inert gas or inactive gas atmosphere or in a vacuum, no oxygen is supplied from the growth environment. The film deposition source must include oxygen. This film deposition category includes a sputtering

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method, a laser deposition method, both of which use a sintered oxide target, an electron beam evaporation method that uses an oxide evaporation source, etc. Since the sputtering method needs a discharge gas, introduction of an argon (Ar) gas of 3N (99.9%) or up in purity by a few mTorr to a few tens of mTorr will do. It should be avoided, however, to use a gas of low purity, since such a gas brings an unexpected result such as unstable discharge, precipitation of impurity phases, etc. The laser deposition method can form oxide films in a vacuum. Of course, no problem will occur if any of inert gasses are used just like in the sputtering method, but it makes no sense principally. Films can also be formed by electron beam deposition method that uses an oxide evaporation source. The vacuum mentioned here is a state achieved by any of evacuation devices without introducing oxidizing gases such as oxygen, nitrogen monoxide, nitrogen dioxide, ozone, etc. intentionally. The pressure should preferably be  $1\mu\text{Torr}$  or under in terms of the non-oxidizing atmosphere in both laser deposition and electron beam deposition methods.

Each of the film deposition methods described above can be applied to form an oxide film on the anti-diffusion non-oxide conductive layer (including a case when the layer is formed via a metallic layer) in a weak oxidizing atmosphere including oxidizing gases such as oxygen,

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nitrogen monoxide, nitrogen dioxide, ozone, etc. slightly. The sputtering method is just required to include an oxidizing gas used as a discharge gas. The laser deposition method is just required to include an oxidizing gas. The electron beam deposition method, when used in a vacuum, can use only an oxide as an evaporation source. When it is used in a weak oxidizing atmosphere, however, it can also use a metal evaporation source. Consequently, the method can use a heater such as an effusion cell (K cell) as a heating source in addition to the electron beam. The pressure should preferably be  $10 \mu\text{Torr}$  or lower in total pressure or partial pressure of the oxidizing gas in use in terms of the non-oxidizing atmosphere in any of the sputtering method, the laser deposition method, and other deposition methods that use an electron beam and a heater.

On the basis of the ideas described above, the following results have been obtained when in checking of the conductive oxides that can satisfy the conditions with respect to the rutile structure, the perovskite structure, and the  $\text{ReO}_3$  structure in which many conductive oxides are known: (a) The resistivity in the room temperature is  $0.01 \Omega\text{cm}$  or lower. (b) Possible to be stabilized in a non-oxidizing atmosphere and under typical conditions (oxygen pressure of  $1 \mu\text{Torr}$  and temperature of  $700^\circ\text{C}$ ).

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In order to satisfy the above requirement (b), it is not desirable that a conductive oxide is composed of multi-valent ion, which are positive center cation. Consequently, conductive oxides including Cr, Mn, Fe, Co, Ni, Cu, and V are excluded.

There are two conductive oxides that crystallized in the rutile structure;  $\text{RuO}_2$  and  $\text{IrO}_2$ .

There are three conductive oxides that crystallized in the perovskite structure;  $\text{CaRuO}_3$  and  $\text{SrRuO}_3$  whose center element is Ru (ruthenium), and (La, Sr)  $\text{TiO}_3$  in which part of Sr of  $\text{SrTiO}_3$  whose center element is Ti (Titanium) is replaced with La by over 0.5 weight % to 4.0 weight % (included) in quantity.

$\text{ReO}_3$  is another conductive oxide that takes the  $\text{ReO}_3$  structure.

When forming a conductive oxide in a non-oxidizing atmosphere, oxygen deficiency is introduced as described above. In the thermal equilibrium state, only slight oxygen deficiency of 0.1% or lower is introduced as a point defect, but film deposition is often made in a non-equilibrium state. Thus, an extra oxygen defect is easily frozen excessively unlike in the thermal equilibrium state. It is very difficult, however, even with the current analysis technique to measure an oxygen defect concentration specific to films. Actually, it is impossible to define an

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A film formed in a non-oxidizing atmosphere will be defined concretely as follows on a condition that the permissible oxygen deficiency allows an objective structure to be kept stable. For the rutile structure, it is defined that an oxygen deficiency  $x$  is larger than 0 and smaller than a value that enables the rutile structure to be kept stable in the chemical formula  $\text{MO}_{2-x}$  with oxygen deficiency in which both Ru and Ir transition elements are represented by M. For the perovskite structure, it is defined that the oxygen deficiency  $x$  is larger than 0 and smaller than a value (upper limit value) that enables the perovskite structure to be kept stable in the chemical formula  $\text{AMO}_{3-x}$  with oxygen deficiency in which both Ru and Ti transition elements are represented by M, and Ca, Sr, and La elements are represented

by A, respectively. At this time, even when an anti-site defect is introduced between cations due to the introduced oxygen deficiency, thereby a lattice constant becomes larger than the standard bulk value, the basic framework is judged to be still within the category of the perovskite structure. For the  $\text{ReO}_3$  structure, it is defined that the oxygen deficiency  $x$  is larger than 0 and smaller than a value that enables the  $\text{ReO}_{3-x}$  structure to be kept stable in the chemical formula  $\text{MO}_{3-x}$  with oxygen deficiency.

The introduction of oxygen deficiency causes the resistivity of the conductive oxide to be increased by almost 10% in maximum, but the conductive oxide is kept low in resistivity enough to be used as electrodes. For example, the resistivity was increased by almost 10% in  $\text{SrRuO}_{3-x}$ , but the resistivity was as small as a few  $\text{m}\Omega\text{cm}$  as an absolute value. In  $\text{IrO}_{2-x}$ ,  $\text{RuO}_{2-x}$ , and  $\text{ReO}_{3-x}$ , the resistivity was increased only to about double in maximum. In other words, it was confirmed that the conductive oxides could keep a resistivity enough to be used for electrodes even when the conductive oxides described above were formed in a non-oxidizing atmosphere.

A possibility of coexistence of decomposed products was as described above when a conductive oxide was formed in a non-oxidizing atmosphere. Both  $\text{RuO}_2$  and  $\text{IrO}_2$  in rutile structures, as well as the  $\text{ReO}_3$  are a monoxide respectively

and each of those structures includes only one type transition element. It is thus no fear that they are decomposed thereby to produce other compounds. On the other hand, the perovskite structure expressed by  $AMO_3$  is a complex oxide which consists of an element M consisting of transition elements and an element A consisting mainly of alkaline-earth metals. It is thus possible that decomposed products coexist at a high temperature of about 700 °C in a non-oxidizing atmosphere. Actually, when Ca was included as an alkaline-earth metal, it was confirmed by an X-ray diffractometer that about a few % CaO existed as a decomposed product. Even when Sr was included, SrO was observed as a decomposed product in a stronger non-oxidizing atmosphere, that is, at a higher temperature and at a lower pressure. In any cases described above, therefore, it was recognized that nothing affected the resistivity in the room temperature. It was concluded from this result that high resistant decomposed products were distributed and coexisted in a conductive oxide, so that a current was flowed in a lower objective conductive oxide.

At a lower temperature than the room temperature, a metallic conduction was observed, where the resistivity was decreased as the temperature was decreased if there was no decomposed product. If decomposed products coexisted, a conduction that caused the resistivity to be increased was

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observed. It was concluded from this result that the increase of the resistivity was caused by the conduction characteristics of decomposed products segregated along grain boundaries in a microscopic fashion.

In any cases described above, at the room temperature or above, the increase of the resistivity caused by coexistence of decomposed products was within an allowable range for conductive oxide layers or semiconductor devices that used conductive oxide layers. In other words, each of conductive oxides that take the perovskite structure may be a mixed phase of  $\text{CaRuO}_3$ ,  $\text{SrRuO}_3$ , and  $(\text{La}, \text{Sr})\text{TiO}_3$  in which a part of Sr of  $\text{SrTiO}_3$  is replaced with La by over 0.5 to 4.0 weight% (included), and an alkaline earthmetal oxide  $\text{CaO}$  or  $\text{SrO}$  composing the subject oxide.

Description has been made so far for the means for achieving the first object of the present invention, that is the characteristics of a semiconductor device, using oxide dielectrics as a capacitor insulator and a double-layered conductive oxide layer as an electrode element, as well as for the means for achieving the second object of the present invention, that is, a method for forming the double-layered conductive oxide layer, selected from the methods for manufacturing such a semiconductor device, and for the means for achieving the third object of the present invention, that is, the characteristics of the double-

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layered conductive oxide layer that can suppress oxygen diffusion and oxidation, and for the means for achieving the fourth object of the present invention, that is, a method for forming the double-layered conductive oxide layer.

Finally, description will be made for the means for achieving the second object of the present invention, that is, a method for manufacturing such a semiconductor device. The method for manufacturing the semiconductor device of the present invention includes processes for forming a lower electrode layer on a substrate as described above with reference to Figs. 1 to 4. The lower electrode layer consists of a polycrystalline silicon layer, a non-oxide conductive layer for anti-diffusion, a metallic layer, and a double-layered conductive oxide layer. Usually, a polycrystalline silicon layer is formed using the chemical vapor deposition. The non-oxide conductive layer for anti-diffusion is formed using the sputtering method, the vacuum deposition method, and the CVD method. The metallic layer is formed using the sputtering method. However, the methods for forming those layers are just examples and they are not limited for modification specially. How to form the double-layered conductive oxide layer is as described in detail. The compound of each layer for composing the lower electrode is also as described above in detail.

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In order to form an oxide dielectric capacitor so that its oxide dielectric layer is between the upper and lower electrode layers, an oxide dielectric layer is formed on this lower electrode layer, then the upper electrode layer is formed on the oxide dielectric layer. Concrete compounds used for forming the oxide dielectric layer are as described above in detail. The sol-gel method with use of alkoxide, the vacuum deposition method, the chemical vapor deposition, the sputtering method, etc. can be used to form the oxide dielectric layer. The methods are not limited only those specially. The upper electrode layer should preferably be formed with the same conductive oxide as that of the lower electrode layer if the symmetry of the current - voltage characteristics of the dielectric capacitor, as well as the symmetry of the polarization hysteresis curve of the ferroelectric capacitor are considered to be important. However, the semiconductor device will work as expected even if the conductive oxide and a noble metal such as platinum, ruthenium, and iridium are different between the upper and lower electrode layers. The upper electrode layer can be formed by any of sputtering, vacuum deposition, sol-gel, and chemical vapor deposition methods. The film deposition method is not limited only to those specially even when a noble metal is used for forming the upper electrode layer.

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Before the oxide dielectric capacitor, that is, the lower electrode layer is formed, part of a MOS transistor is formed on the substrate. The source area or the drain area of the MOS transistor is connected electrically to the lower electrode layer through the conductive material filled in the contact holes formed through the insulator, which covers the semiconductor substrate on which the MOS transistor itself is formed. Polycrystalline silicon formed using the chemical vapor deposition is often used as the conductive material filled in these contact holes. The polycrystalline silicon deposition method and the filling material are not limited only those specially.

## 2. Guideline 2 for Selecting Conductive Materials

This guideline is determined to achieve the first and second objects of the present invention, especially on the basis of the configuration of (the conventional technology 7).

In order to achieve the first object of the present invention, the semiconductor device of the present invention is provided with an oxide dielectric capacitors formed on a semiconductor substrate. The capacitor consists of a lower electrode layer including an aluminum titanium nitride layer, an oxide dielectric layer formed on the aluminum titanium nitride layer, and an upper electrode layer formed on the oxide dielectric layer. Figs.5 and 6

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show two typical cross sectional views of the lower electrode layer. Figs.5 and 6 do not show any detailed structure of the oxide dielectric capacitor provided in the semiconductor device of the present invention, but they show simplified views of how each layer of the capacitor is stacked.

In Fig.5, the lower electrode layer 11 consists of the aluminum titanium nitride layer 50 formed on the polycrystalline silicon layer 20, and the metallic layer 40 formed further on the layer 50. The conductive polycrystalline silicon layer 20 corresponds to the first area described above in the concept of the semiconductor device. The aluminum titanium nitride layer 50 corresponds to the second area described above in the concept of the semiconductor device. The metallic layer 40 corresponds to the third area described above in the concept of the semiconductor device. In Fig.6, a conductive oxide layer 60 is stacked on the component of the lower electrode layer 11 shown in Fig.5. This conductive oxide layer 60 corresponds to an area provided between the third and fourth areas described above in the concept of the semiconductor device.

The lower electrode layer 11 is also connected electrically to a predetermined area of the semiconductor

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Hereunder, the function of the aluminum titanium nitride layer 50 used for preventing oxygen diffusion and oxidation will be described. As described in the conventional technologies, the titanium nitride layer used as a layer for preventing oxygen diffusion and oxidation, which have been examined so far, is weak in anti-reaction to oxygen. And, in order to compensate this weak point of the titanium nitride layer, it is indispensable to put a metallic layer made of platinum, etc. therebetween. A platinum of about 200nm in thickness is also needed to secure a time of oxygen diffusion at grain boundaries in platinum. On the other hand, the titanium nitride layer still has attraction, since it acts to prevent oxidization to a certain level while it keeps a high conductivity. This is why aluminum is added to titanium nitride to obtain a remarkable resistance to oxidization. The resistance was found as a result of examination for the possibility of improvement of the resistance to oxidization by adding the second metallic element to titanium nitride.

The reaction of a nitride to oxidization, thereby to be changed into an oxide, is considered to be a reaction that substitute oxygen with nitrogen in the nitride. In other words, it may be considered that the height of the energy

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barrier between the nitride and the oxide dominates this substitution qualitatively. In the aluminum titanium nitride obtained by the present invention, the improvement of the anti-reaction to oxygen is considered to be caused by this heightened energy barrier. Regardless of this chemical background, however, it was found that the aluminum titanium nitride could function enough as an anti-oxidizing layer if part of titanium in the titanium nitride is replaced with aluminum. In terms of this anti-oxidizing property, if the chemical formula of the aluminum titanium nitride was expressed by  $(\text{Ti}_{1-x}\text{Al}_x)_{1-y}\text{N}_y$ ,  $x$  should preferably be 0.2 or above and  $y$  should preferably be 0.4 or above. If  $x$  is smaller than 0.2, the anti-oxidizing property is not improved at all. If  $y$  is smaller than 0.4,  $\text{TiO}_2$  produced by oxidation is observed in an X-ray diffraction measurement.

Aluminum nitride is a high resistant material. If part of titanium is replaced with aluminum, the resistivity increases. If such aluminum titanium is to be used for each electrode of a semiconductor device, the resistivity should preferably be  $10\text{m } \Omega\text{cm}$  or under. Consequently, if aluminum titanium nitride is represented by a chemical formula of  $(\text{Ti}_{1-x}\text{Al}_x)_{1-y}\text{N}_y$ ,  $x$  should preferably be 0.5 or below and  $y$  should preferably be between 0.4 and 0.6. If an impurity phase is precipitated, the material becomes inhomogeneous

in the electrode, thereby forming of fine-integrated memory cells is disabled. In order to avoid this, the x value should preferably be 0.6 or below and the y value should preferably be 0.2 or above, and 0.6 or below.

In conclusion, the x value should preferably be 0.2 or above, and 0.5 or below and the y value should preferably be 0.4 or above, and 0.6 or below in the aluminum titanium nitride expressed by a chemical formula of  $(\text{Ti}_{1-x}\text{Al}_x)_{1-y}\text{N}_y$ .

Another requirement for the aluminum titanium nitride layer, that is, the property of anti-diffusion is expected to be equivalent to that in the titanium nitride layer, since the structure of titanium nitride which is a mother compound is maintained, intrinsically. Thus, no problem is found specially from the layer.

The metallic layer 40 covering the aluminum titanium nitride layer shown in Figs.5 and 6 should preferably be at least one of noble metals excellent in anti-oxidizing properties, that is, platinum, iridium, and ruthenium. For the conventional structure in which the anti-oxidizing layer is made of titanium nitride, the metallic layer had to be about 200nm in thickness. For the aluminum titanium nitride layer of the present invention, the resistance to oxidation is already improved. For example, 30nm will do as the thickness of the metallic layer as long as the layer

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can cover the surface of the aluminum titanium nitride layer completely.

For the structure shown in Fig.5, an oxide dielectric layer 16 is formed on the metallic layer 40. However, a conductive oxide layer 60 may be inserted between the oxide dielectric layer 16 and the metallic layer 40 as a component of the lower electrode layer. The conditions for forming a conductive oxide layer in an oxidizing atmosphere are usually the same as those of forming an oxide dielectric layer. Thus, it may be considered that the resistance to oxidization required for the aluminum titanium nitride layer is also the same. Since such a conductive oxide layer can improve the contact property at each interface with a metallic layer, if it includes the same elements of a noble metal as those of the metallic layer, it should preferably be at least one of  $\text{IrO}_2$ ,  $\text{RuO}_2$ ,  $\text{SrRuO}_3$ , and  $\text{ReO}_3$ .

Hereunder, preferred materials for the oxide dielectric layer 16 will be described. There is no reason to limit the materials for the layer 16 specially. The following materials usable for the layer 16 are well known. Typical examples of oxide dielectrics whose center element is titanium are lead zirconate titanate obtained by replacing part or whole of titanium with zirconium, lead barium zirconate titanate obtained by replacing part or whole of the lead with barium, barium strontium titanate

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including only alkaline-earth metal elements, etc. As typical examples of bismuth dielectrics with layered structure, there are bismuth layered dielectrics such as  $\text{Bi}_4\text{Ti}_3\text{O}_{12}$ ,  $\text{SrBi}_2\text{Ta}_2\text{O}_9$ , etc. In addition to those examples, other well-known oxide dielectrics, oxide ferroelectrics, and new oxide dielectrics and oxide ferroelectrics to be discovered in the future are all usable as the oxide dielectric layer described above.

The upper electrode layer 17 may be any material if it is conductive. They are not limited only to metals and oxides. Each of the noble metals described above (in the example of the metallic layer 40 provided in the lower electrode layer) is usable. Each of the oxides described above (in the example of the conductive oxide layer 60 provided in the lower electrode layer) is usable. The materials of the upper electrode layer 17 are not limited only to those specially.

Next, description will be made for a method for manufacturing the semiconductor device of the present invention in order to achieve the second object described above. The method for manufacturing the semiconductor device of the present invention includes a process for forming the lower electrode layer including an anti-diffusion and anti-oxidation layer of aluminum titanium nitride which is formed in a nitriding atmosphere using the



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sputtering method. Various types of sputtering targets are usable; for example, a metallic target consisting of a titanium aluminum alloy, a composite-target obtained by putting an aluminum metal or aluminum nitride on a titanium target, a composite-target obtained by putting a titanium metal or a titanium nitride on an aluminum target, a dual target consisting of a titanium target and a aluminum target and so as to be sputtered simultaneously, a nitride target consisting of an aluminum titanium nitride, a composite-target obtained by putting an aluminum metal or an aluminum nitride on a titanium nitride target, a composite-target obtained by putting a titanium metal or a titanium nitride on a aluminum nitride target, a dual target consisting of an aluminum nitride target and a titanium nitride target separately and so as to be sputtered simultaneously, etc. Any of DC and AC can be used for the sputtering discharge. If an aluminum nitride whose resistance is large is used as a target, however, an RF discharging is required.

At least, a discharge gas and a nitrogen gas must be included in the atmosphere used for forming an anti-diffusion and anti-oxidation layer of aluminum titanium nitride. A inert gas can be used as a discharge gas. However, usually an argon gas is used considering the economy. A nitrogen gas is included in the discharge gas by 10 to 90 mole%, since it requires sufficient nitridation

and a high through-put (high deposition rate). If there is no restriction for both semiconductor device and environment, a few percent ammonia gas may be included thereby to accelerate nitridation and suppress oxidation.

The temperature should preferably be above the room temperature to 600 °C (included) when a aluminum titanium nitride anti-diffusion and an anti-oxidation layer are to be formed with the sputtering method. Of course, the room temperature does not mean that samples are kept in the room temperature, but it means that the samples should not be cooled or heated specially. Natural rising of the temperature should be allowed during the sputtering. When a sample was formed at a temperature above 600 °C in a heating process, it was observed by an X-ray diffraction measurement that an aluminum nitride (AlN) was generated separately from the sample.

Furthermore, in order to achieve the second object described above, the method for manufacturing the semiconductor device of the present invention includes a process for completing the lower electrode layer by stacking a metal layer, or a metal layer and a conductive oxide layer sequentially on an anti-diffusion and anti-oxidation layer of aluminum titanium nitride. On this lower electrode layer, an oxide dielectric layer is formed. Then, the upper electrode layer is stacked thereon so that an oxide

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dielectric capacitor is formed in a structure so that the oxide dielectric layer is put between the upper and lower electrode layers. The metallic layer may be formed with any of the sputtering method, the vacuum evaporation method, etc. As for the conductive oxide layer and the oxide dielectric layer, the sputtering method, the reactive evaporation method, the laser ablation method, the chemical vapor deposition method, the sol-gel method, etc. are usable. The method is not limited specially. The upper electrode layer may also be formed with any of those methods.

Before the oxide dielectric capacitor, that is, the lower electrode layer is formed, part of a MOS transistor is formed on the substrate. The lower electrode layer is connected electrically to the source area or the drain area of this MOS transistor through the conductive material filled in the contact holes perforated in the insulator, which covers the semiconductor substrate on which the MOS transistor itself is formed. Polycrystalline silicon formed using the chemical vapor deposition method is often used as the conductive material filled in these contact holes. The forming method and the filling material are not limited specially.

### 3. Characteristics of the Semiconductor Device of the Present Invention

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The semiconductor device to be realized by an embodiment of the present invention on the basis of the above two guidelines for selecting conductive materials will have the following characteristics.

The semiconductor device of the present invention is provided with the first area (a semiconductor substrate or a semiconductor film, etc.) consisting of a conductive semiconductor material, the second area connected to the first area and consisting of the first conductive material, the third area connected to the second area and consisting of the second conductive material, the fourth area connected to the third area and consisting of an oxide dielectrics, and the fifth area connected to the fourth area and consisting of a conductive material. And, the average resistivity of the first area is almost equal to the resistivity of the semiconductor material composing the first area and the average resistivity of the second area is almost equal to the resistivity of the first conductive material composing the second area. Such the characteristics mean that the respective electric resistances of the first to third areas are determined uniquely by the resistivity of the semiconductor material or the conductive material used for forming each of those areas, as well as by the length of the current path in each of those areas (or the thickness of each of those areas, if

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it is stacked vertically). In other words, the embodiment of the present invention can avoid the forming of a high resistant material almost completely in the first or second area, which has been a problem of the conventional technology. And accordingly, it is possible to suppress an increase of the electrical resistance in those areas, as well as enabling the average resistivity in the current path from the first area to the third area to be set  $0.01 \Omega\text{cm}$  or below.

Consequently, according to the present invention, when both oxide dielectric layer and conductive oxide layer are formed, memory cells can be formed without oxidizing the polycrystalline silicon layer adjacent to both oxide dielectric layer and conductive oxide layer, as well as the anti-diffusion non-oxide conductive layer consisting of a nitride, etc. Consequently, it becomes possible to reduce both interfacial resistance and contact resistance of each electrode, obtaining a semiconductor device provided with fine-structured memory cells, suitable for high integration. In addition, the semiconductor device of the present invention can omit a process for forming a metallic layer of 200nm or over in thickness consisting of platinum and the like as an anti-oxidizing layer, as well as it can reduce the total thickness and the aspect ratio of the capacitor by thinning the lower electrode layer. It is thus

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possible for the present invention to obtain a semiconductor device provided with fined-structured memory cells to be formed through a fine-patterned process of                      submicron region, for example, using a gigabit class lithographic technology.

#### Brief Description of the Invention

Fig.1 illustrates an oxide dielectric capacitor provided with a double-layered conductive oxide layer included in its lower electrode layer.

Fig.2 illustrates an oxide dielectric capacitor provided with a double-layered conductive oxide layer formed on a polycrystalline silicon layer.

Fig.3 illustrates an oxide dielectric capacitor provided with a double-layered conductive oxide layer formed on an anti-diffusion non-oxide conductive layer.

Fig.4 illustrates an oxide                      dielectric capacitor provided with a double-layered conductive oxide layer formed on an anti-diffusion non-oxide conductive layer through a metallic layer.

Fig.5 illustrates an oxide dielectric capacitor provided with an oxide dielectric layer on a metallic layer stacked on an aluminum titanium nitride layer.

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titanium nitride layer. (a) indicates a case that an oxide dielectric layer stacked on a metallic layer and (b) indicates a case that an oxide dielectric layer is stacked on a conductive oxide layer.

Fig. 12 illustrates a manufacturing process of the semiconductor device of the present invention in an embodiment.

Fig. 13 illustrates a manufacturing process of the semiconductor device of the present invention in an embodiment.

Fig. 14 illustrates a manufacturing process of the semiconductor device of the present invention in an embodiment.

Fig. 15 illustrates manufacturing process of the semiconductor device of the present invention up to a planarizing process in an embodiment.

Fig. 16 illustrates a manufacturing process of the semiconductor device in which a double-layered conductive oxide layer is formed on a polycrystalline silicon layer.

Fig. 17 illustrates a manufacturing process of the semiconductor device in which a double-layered conductive oxide layer is formed on an anti-diffusion non-oxide conductive layer.

Fig. 18 illustrates a manufacturing process of the semiconductor device in which a double-layered conductive

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oxide layer is formed on an anti-diffusion non-oxide conductive layer through a metallic layer.

Fig. 19 illustrates a manufacturing process of the semiconductor device which is provided with an aluminum titanium nitride layer formed so as to form an oxide dielectric layer on a metallic layer.

Fig. 20 illustrates a manufacturing process of the semiconductor device which is provided with an aluminum titanium nitride layer formed so as to form an oxide dielectric layer on a conductive oxide layer. Fig. 20 also indicates a cross sectional structure of a scribing area of a silicon wafer in the eighth embodiment of the present invention.

#### Best mode for Carrying out the Invention

Hereunder, the preferred embodiments of the present invention will be described. How to form a capacitor using oxide dielectrics and how to apply the capacitor to an actual semiconductor device will be described separately. The former way is further described by the conductive material selection guideline described above.

##### 1. How to Form an Oxide Dielectric Capacitor

###### 1-1 Guideline 1 for selecting conductive materials

At first, description will be made for the first to third preferred embodiments of the present invention with

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reference to the accompanying drawings if a double-layered conductive oxide layer is selected for two conductive oxide layers provided between a semiconductor layer and a dielectric layer in an electrode of an oxide dielectric capacitor suitable for a semiconductor device.

<First Embodiment>

In the first embodiment of the present invention, the resistance of the lower electrode layer and the polarization hysteresis curve of an oxide ferroelectric capacitor were measured with respect to the lower electrode layer 11 formed so as to form a conductive oxide layer 14 with oxygen deficiency in a double-layered conductive oxide layer 12 shown in Fig.2 directly on a polycrystalline silicon layer 20.

At first, an amorphous silicon layer doped with phosphorus of 150nm in thickness was formed on a 15mm square conductive silicon substrate 10 by the chemical vapor deposition. The substrate was then annealed thereby obtaining a conductive polycrystalline silicon layer 20. Then, two types of samples were formed on this substrate. One sample was formed as follows; at first, conductive oxide layers 14 and 15 were formed through a 2mm square metal mask, then they were further shrunk down to a 100  $\mu$ m square by electron beam lithography. This sample was used for measuring the resistance of the object electrode. The other

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sample was formed as follows; at first, conductive oxide layers 14 and 15 were formed on the entire surface of the substrate, then an oxide dielectric layer 16 and the upper electrode layer 17 were stacked like a pyramid through a 4mm square metal mask and another metal mask of 2mm in diameter, respectively. Then, the upper electrode layer 17 was shrunk down to a  $10\mu\text{m}$  square by ion milling using a photo mask. This sample was used for measuring the characteristics of the object capacitor.

To form the conductive oxide layers 14 and 15,  $\text{IrO}_2$ ,  $\text{RuO}_2$ ,  $\text{SrRuO}_3$ ,  $\text{SrTiO}_3$  to which La was added by 4 weight%, and  $\text{ReO}_3$  were used (in this embodiment, chemical formulas are used to clarify each compound. The description of the oxygen deficiency is omitted for convenience's sake). Next, how to form each oxide layer will be described. However, the methods described here for manufacturing each compound are just examples. They may be exchanged by each other.

The electron beam deposition method was used only for forming  $\text{IrO}_2$ . At first, the  $\text{IrO}_2$  oxide powder was molded into a cylinder shape of 12mm in diameter and 10mm in thickness using a pressure die. After this, it was annealed at  $1100^\circ\text{C}$  for 2 hours in an oxygen gas flow. This was used as an electron beam source. Then, a  $\text{IrO}_2$  layer with oxygen deficiency was formed under the following conditions: temperature of the substrate heater;  $600^\circ\text{C}$ , deposition

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rate; 2nm/min, and pressure; 0.1  $\mu$ Torr. After this, oxygen gas was introduced up to a pressure of 70  $\mu$ Torr. At the same time, the substrate heater was set to 580  $^{\circ}$ C thereby stacking a 50nm  $\text{IrO}_2$  layer to obtain a double-layered conductive oxide layer 12.

The conductive oxide layers other than  $\text{IrO}_2$  were formed by the RF-magnetron sputtering method using a sintered oxide target consisting of the above cation composition. An oxide dielectric layer of 5 to 50nm in thickness with oxygen deficiency was formed on the following film deposition conditions: temperature of the substrate heater; 600  $^{\circ}$ C, incident power; 1.5W/cm<sup>2</sup>, deposition rate; 3nm/min, and discharge Ar gas pressure of 3N in purity; 3 mTorr. After this, oxygen was introduced at  $\text{Ar/O}_2=9/1$  and the substrate heater was set to 580  $^{\circ}$ C, thereby forming a conductive oxide layer so as to form a double-layered conductive oxide layer 12.

The oxide dielectric layer 16 was formed using the RF-magnetron sputtering method using bismuth titanate ( $\text{Bi}_4\text{Ti}_3\text{O}_{12}$ ), which is one of bismuth layered ferroelectrics. The target was a sintered material represented by the above cation composition. The film deposition conditions are as follows: temperature of the substrate heater; 600  $^{\circ}$ C, discharge gas/oxygen gas pressure ratio;  $\text{Ar/O}_2=9/1$ , total pressure; 5 mTorr, incident power; 1.5W/cm<sup>2</sup>, deposition

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rate; 5nm/min, and thickness; 200nm. The type and preparation method of the oxide dielectric layer just affected the substantial physical properties of the capacitor. There was recognized no influence on the double-layered conductive oxide layer. On the upper electrode layer 17 was deposited a gold film of 100nm in thickness using the electron beam deposition method.

Fig. 7(a) shows the total resistance (vertical axis) of the entire lower electrode layer as a function of the thickness (horizontal axis) of the conductive oxide layer with oxygen deficiency, formed in a non-oxidizing atmosphere. The resistance was measured between the conductive oxide layer formed in an oxidizing atmosphere and the conductive silicon substrate. In any conductive oxide electrodes, if the oxygen deficient layer was 5nm in thickness, the electrode resistance was very large. Thus, it was clear that polycrystal silicon was oxidized, thereby increasing the resistance. If the oxygen deficient layer was 5 to 10nm in thickness, the resistance dropped sharply and the layer was 10nm or over in thickness, then the resistance was almost constant. From this result, it was clear that the covering ratio of the surface of the polycrystal silicon increased and that the oxidation of the polycrystal silicon was suppressed. It was because of a resistivity difference affected on the conductive oxide

The resistivity of a conductive oxide material itself, when measured for another single layer film, was only a few tens of  $\mu\Omega\text{cm}$  or so for  $\text{IrO}_2$ ,  $\text{RuO}_2$ , and  $\text{RuO}_3$  and as low as two or three times of that even in the oxygen deficient film. As for  $\text{SrRuO}_3$ , if oxygen deficiency was introduced, the resistivity increased just within  $200\mu\Omega\text{cm}$  to a few  $\text{m}\Omega\text{cm}$ . For  $\text{SrTiO}_3$  to which La was added by 4 weight%, the resistivity increased within a few hundreds of  $\mu\Omega\text{cm}$  to a few  $\text{m}\Omega\text{cm}$ . These results matched with the tendency shown in Fig.7(a) and indicated that the resistivity did not increase remarkably even when the double-layered conductive oxide electrode grew adjacent to the polycrystalline silicon.

Fig. 7(b) shows a polarization hysteresis curve of an oxide ferroelectric capacitor that uses oxide electrodes when the oxygen deficient layer is 30nm in thickness. There is no difference in the hysteresis curve between the types of oxide electrodes. As shown clearly in Fig. 7(b), if a conductive oxide layer adjacent to polycrystalline silicon is formed in a non-oxidizing atmosphere, both oxidation and oxygen diffusion are suppressed. It is thus possible to prove that a voltage supplied from the substrate can be applied effectively to the oxide dielectric layer.

### <Second Embodiment>

In the second embodiment of the present invention, the resistance of the lower electrode layer and the polarization hysteresis curve of the oxide ferroelectric capacitor were measured with respect to the structure of the lower electrode layer 11. In the lower electrode layer 11 provided in the double-layered conductive oxide layer 12 shown in Fig. 3, the conductive oxide layer 14 with oxygen deficiency, is formed on a conductive nitride layer which functions as an anti-diffusion non-oxide conductive layer 30.

At first, an amorphous silicon film with a thickness of 150nm was formed on the 15mm square conductive silicon substrate 10 using the chemical vapor deposition while doping phosphorus. Then, the amorphous silicon film was annealed thereby to form a conductive polycrystalline silicon layer 20. After this, a conductive nitride layer, which would function as an anti-diffusion non-oxide conductive layer 30, was formed all over the substrate. On this ground layer was formed two types of samples. One sample was formed as follows; conductive oxide layers 14 and 15 were formed through a 2mm square metallic mask, then the layers 14 and 15 were shrunken down to a 100  $\mu$ m square respectively by electron beam lithography. The sample was used for measuring electrode resistance. The other sample was formed as follows; conductive oxide layers 14 and 15 were formed all over the surface of the substrate, then an oxide

dielectric layer 16 and an upper electrode layer 17 were stacked like a pyramid through a 4mm square metallic mask and a 2mm diameter metallic mask, respectively, and further the upper electrode layer 17 was shrunken down to a 10  $\mu$ m square by electron beam lithography. The sample was used for measuring capacitor characteristics.

In this embodiment, TiN and TaN were used as conductive nitride layer (anti-diffusion non-oxide conductive layer 30), which will be described below in detail. The film deposition method and the obtained results were also the same with respect to Zr, Nb, V, and W nitrides. A conductive nitride layer was formed using the DC sputtering method that used a metal target. The film deposition conditions were as follows: temperature of the substrate heater; 300 °C, discharge gas/nitrogen gas pressure ratio; Ar/N<sub>2</sub> = 50/50, total pressure; 4 mTorr, incident power; 400W, and film thickness: 40nm. The RF-magnetron sputtering method can also be used for forming the conductive nitride layer. The method may use a nitride target instead of the metallic target. After the film deposition, an annealing treatment was applied to the sample so as to accelerate crystallization using the rapid thermal annealing method at 800 °C for two minutes in an ammonia gas atmosphere.



For the conductive oxide layers 14 and 15, compounds of  $\text{IrO}_2$ ,  $\text{RuO}_2$ ,  $\text{SrRuO}_3$ ,  $\text{CaRuO}_3$  and  $\text{ReO}_3$  were used respectively. (Chemical formula were just used to clarify each compound here. The description of the amount of oxygen deficiency was omitted for the convenience's sake.) Each oxide layer was formed as follows. Each deposition method described here was just an example. The deposition method could also be replaced with another.

The compound  $\text{IrO}_2$  were formed in a weak oxidizing atmosphere using the RF-magnetron sputtering method. The target was a sintered oxide one. The film deposition conditions were as follows: temperature of the substrate heater;  $600^\circ\text{C}$ , incident power;  $1.5\text{W}/\text{cm}^2$ , discharge gas; Ar gas of 3N in purity and 3 mTorr in pressure, and weak oxidizing gas;  $\text{N}_2\text{O}$  gas of  $\text{Ar}/\text{N}_2\text{O}=100/1$  in flow ratio. Under those conditions, a conductive oxide layer with oxygen deficiency was formed with a film thickness of 5 to 50nm. Then, the gas flow ratio was lowered to  $\text{Ar}/\text{N}_2\text{O}=9/1$ , as well as the total pressure was set to 5 mTorr and the temperature of the substrate heater was set to  $580^\circ\text{C}$  to form a 50nm conductive oxide layer, thereby forming a double-layered conductive oxide layer 12.

$\text{SrRuO}_3$  and  $\text{CaRuO}_3$  were formed in an Ar gas atmosphere using the RF-magnetron sputtering method that used a sintered oxide target. The film deposition conditions were

as follows: temperature of the substrate heater; 600 °C, incident power; 1.5W/cm<sup>2</sup>, and discharge gas; Ar gas of 3N in purity and 3 mTorr in pressure. Under those conditions, a conductive oxide layer with oxygen deficiency was formed with a film thickness of 5 to 50nm. Then, oxygen was introduced at a gas flow ratio of Ar/O<sub>2</sub>=9/1, as well as the total pressure was set to 5 mTorr and the temperature of the substrate heater was set to 580 °C to form a 50nm conductive oxide layer, thereby forming a double-layered conductive oxide layer 12.

RuO<sub>2</sub> and ReO<sub>3</sub> were formed in a weak oxidizing atmosphere using the reactive evaporation method. A metal block was used as the evaporation source. The film deposition conditions were as follows: temperature of the substrate heater; 600 °C, deposition rate; 1 nm/min, and oxygen pressure; 5 μTorr. Under those conditions, an oxygen deficient layer was formed with a thickness of 5 to 50nm, then oxygen was introduced at a pressure up to 70 μTorr, as well as the temperature of the substrate heater was lowered to 580 °C thereby to stack the 50nm thick RuO<sub>2</sub> and ReO<sub>3</sub> layers, so that a double-layered conductive oxide layer 12 was formed.

For the oxide dielectric layer 16, lead zirconate titanate [Pb(Zr<sub>0.5</sub>Ti<sub>0.5</sub>)O<sub>3</sub>] was used. The RF-magnetron sputtering method was used to form the layer 16. The target

was a sintered one represented by the above cationic composition. The film deposition conditions were as follows: temperature of the substrate heater; 600 °C, discharge gas/oxygen gas pressure ratio;  $\text{Ar}/\text{O}_2 = 9/1$ , total pressure; 5 mTorr, incident power;  $1.5\text{W}/\text{cm}^2$ , deposition rate; 5 nm/min, and film thickness; 200nm. The type and film deposition method of the oxide dielectric layer affected only the substantial physical characteristics of the capacitor and did not affect the double-layered conductive oxide film. The upper electrode layer 17 was formed with the same conductive oxide as that of the lower electrode layer in an oxidizing atmosphere using the RF-magnetron sputtering method. The film thickness was 80nm.

TiN ((a) in Fig.8) and TaN ((b) in Fig.8) were used respectively for forming the anti-diffusion non-oxide conductive layer 30. The resistance (vertical axis) of the entire lower electrode layer was shown as a function of the thickness (horizontal axis) of the oxygen deficient layer. The resistance was measured between the conductive oxide layer formed in an oxidizing atmosphere and the conductive silicon substrate. The resistance depended on the thickness of the oxygen deficient layer in the same way as the above regardless of the type, deposition method, and deposition conditions of the nitride layer and the conductive oxide electrode. The electrode resistance was significantly high

when the oxygen deficient layer was 5nm in thickness. This was because the interface was oxidized, thereby the resistance was increased when the coating ratio of the nitride layer surface was small and a conductive oxide layer was formed in the subsequent oxidizing atmosphere. The resistance was reduced sharply as the thickness was between 5nm and 10nm and almost constant at 10nm or over. This was because the coating rate of the nitride layer surface was increased, thereby the oxidization of the phase boundary was suppressed. The reason why the resistance was high when using  $\text{CaRuO}_3$  for an oxide electrode was an increase of the contact resistance at the electrode interface. This was confirmed using the X ray diffraction method. As for an electrode including  $\text{IrO}_2$ ,  $\text{RuO}_2$ , and  $\text{ReO}_3$  layers formed in weak-oxidizing atmosphere, the resistance was slightly larger than that of an electrode including  $\text{SrRuO}_3$  formed in the Ar gas. In any compounds, it was clear that the resistance was kept low enough to be used for the object electrode layer. The resistivity of a conductive oxide material itself was as described in the first embodiment of the present invention when measured for the respective single layer film of  $\text{IrO}_2$ ,  $\text{RuO}_2$ ,  $\text{ReO}_3$ ,  $\text{SrRuO}_3$ , and  $\text{SrTiO}_3$  obtained by adding La by 4 weight%. The resistivity of the  $\text{CaRuO}_3$ , when the film was formed in a non-oxidizing atmosphere, increased up to a little less than several

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hundreds of  $\mu\Omega\text{cm}$  to  $10\text{ m}\Omega\text{cm}$ . These results coincide with the tendency shown in Fig. 8(a), indicating that the resistance did not increase so much even when the double-layered conductive oxide electrodes grew in adjacent to the anti-diffusion non-oxide conductive layer 30.

Fig. 8(c) shows a polarization hysteresis curve of an oxide ferroelectric capacitor when the oxygen deficient layer is 10nm in thickness in a case that TiN is used as a nitride layer. For an electrode that includes a  $\text{CaRuO}_3$  layer, the hysteresis curve is opened to the horizontal axis more than those of other electrodes. This seems to be because of the decomposed CaO causes the distribution in the electric field which is applied to dielectrics. However, there is no problem, since characteristics are good enough for the capacitor. As shown in Fig. 8(c) clearly, it is proved that if a conductive oxide layer is formed adjacent to a nitride layer in a non-oxidizing atmosphere, both oxidation and oxygen diffusion are suppressed, thereby a voltage can be applied to the oxide dielectric layer effectively from the substrate. The same hysteresis curve as that shown in Fig. 8(c) was also obtained for the TaN layer.

<Third Embodiment>

In the third embodiment of the present invention, the polarization hysteresis curve for an oxide ferroelectric

capacitor was measured with respect to the structure of the lower electrode layer 11, in which the conductive oxide layer 14 with oxygen deficiency is formed on an anti-diffusion non-oxide conductive layer 30 via metallic layer 40. The layer 14 is provided in the double-layered conductive oxide layer 12 shown in Fig. 4.

The shapes and film deposition methods of the substrate 10, the polycrystalline silicon layer 20, a TiN layer or the anti-diffusion non-oxide conductive layer 30, as well as the oxide dielectric layer 16 and the upper electrode layer 17 are the same as those in the first and second embodiments described above. It is not essential to select the materials of the oxide dielectric layer and the upper electrode layer, however in the embodiments of the present invention.

The TiN layer was formed with a thickness of 40nm in accordance with the method of the second embodiment. The TiN layer was used as an anti-diffusion non-oxide conductive layer 30. The same results were also obtained for other nitrides listed in the above second embodiment.

In this embodiment, platinum was used for the metallic layer 40. The same effect was also found when iridium and ruthenium, which are the same nobles metals as platinum, were used. The DC sputtering method was used for forming the metallic layer on the following conditions: Incident

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power; 400W, discharge gas; Ar, gas pressure; 20 mTorr, and temperature of the substrate heater: 500 °C. The metallic layer 40 was thus formed with a thickness of 20nm on the whole area of anti-diffusion non-oxide conductive layer 30.

$\text{IrO}_2$ ,  $\text{RuO}_2$ ,  $\text{SrRuO}_3$ , and  $\text{SrTiO}_3$  to which La was added by 4 weight% were used for forming the conductive oxide layer using the RF-magnetron sputtering method in a weak oxidizing atmosphere. The targets were a sintered oxide one respectively. The film deposition conditions were as follows: temperature of the substrate heater; 600 °C, incident power; 1.5W/cm<sup>2</sup>, discharge gas; Ar gas of 3N in purity and 3 mTorr in pressure, and weak oxidizing gas;  $\text{N}_2\text{O}$  gas of  $\text{Ar}/\text{N}_2\text{O}=100/1$  in flow ratio. Under these conditions, the conductive oxide layer 14 with oxygen deficient layer of 10nm in thickness was formed. Then, the gas flow ratio was lowered to  $\text{Ar}/\text{N}_2\text{O}=9/1$ , as well as the total pressure was set to 5 mTorr and the substrate heater was set to 580 °C to form a 50nm thick conductive oxide layer 15, thereby forming a double-layered conductive oxide layer 12.

Fig.9 shows a polarization hysteresis curve of an oxide ferroelectric capacitor with respect to each conductor oxide. Regardless of the oxygen deficient layer type, the hysteresis curve was an opened one with high symmetry. Even when the metallic layer was as thin as 20nm and a conductor oxide layer adjacent to this metallic layer

was formed in a weak oxidizing atmosphere, the oxygen deficient layer included in the conductive oxide layer was found to be effective for suppressing oxidation and oxygen diffusion, thereby a voltage could be applied effectively to the oxide dielectric layer from the substrate.

As described above in each of the embodiments of the present invention, a conductive oxide layer with oxygen deficiency was formed in a non-oxidizing atmosphere, which is one of the characteristics of the present invention, thereby forming a double-layered conductive oxide layer. Consequently, the lower electrode layer and the oxide dielectric layer could be formed without oxidizing the polycrystalline silicon (the first embodiment of the present invention) adjacent to the double-layered conductive oxide layer, the anti-diffusion non-oxide conductive layer consisting of an nitrides, etc. adjacent to the double-layered conductive oxide layer, as well as the anti-diffusion non-oxide conductive layer (the second embodiment of the present invention) adjacent to the double-layered conductive oxide layer through a metallic layer. Consequently, it was possible to reduce the interfacial resistance and contact resistance of each electrode, thereby forming an oxide dielectric capacitor suitable for high integration.

1-2 Guideline 2 for Selecting Conductive Materials

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Hereunder, description will be made for how to select an aluminum titanium nitride layer at the side of the semiconductor and an anti-oxidization metallic layer at the side of the dielectrics of the two conductive material layers provided between a semiconductor layer and a dielectric layer in the electrode of an oxide dielectric capacitor suitable for a semiconductor device. The accompanying drawings will be referenced for describing the fourth and fifth embodiments of the present invention.

<Fourth Embodiment>

In the fourth embodiment of the present invention, the allowable contents of both aluminum and nitrogen were checked in an aluminum titanium layer with respect to the phase uniformity, low resistivity, and resistance to oxidation. The phase uniformity and the resistance to oxidation were checked by the X ray diffraction method and the resistivity was measured using the DC four-point probe method.

At first, an aluminum titanium nitride  $[(Ti_{1-x}Al_x)_{1-y}N_y]$  film was formed on a conductive silicon substrate using the DC sputtering method. A natural oxidized film was already removed from the substrate before this deposition. The target was a composite one obtained by spreading aluminum and titanium metallic plates in a mosaic fashion all over an aluminum metal plate. The aluminum content  $x$  was adjusted

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according to the area ratio of both metallic plates. The nitrogen content  $y$  was adjusted by changing the argon discharge gas/nitrogen gas flow ratio within the range of 95/5 to 5/95. The substrate heater was set to 550 °C. Other film deposition conditions were as follows: Incident power; 400W, total gas pressure; 5 to 20 mTorr, growth rate; 5 to 10 nm/min, and film thickness; 50nm. The aluminum content  $x$  was analyzed and determined using the ICPS method (Inductively-Coupled Plasma Spectroscopy) and the nitrogen content  $y$  was analyzed and determined using the RBS (Rutherford Back Scattering) method that uses  $\text{He}^+$  ions.

Fig. 10(a) shows both reaction products and resistivity of a sample whose nitrogen content  $y$  is 0.5 as a function of the aluminum content  $x$ . As a result of X ray diffraction, only a diffraction line assignable to TiN was observed when  $x$  was 0.6 or below. If  $x$  exceeded 0.6, however, a mixed phase with a phase assignable to AlN was observed. As the  $x$  value increased, the TiN phase disappeared and the AlN phase increased. The resistivity increased a little as the  $x$  value increased. The resistivity increased sharply around 0.5. Fig. 10(b) shows both reaction products and resistivity of a sample whose aluminum content  $X$  is 0.4 as a function of the nitrogen content  $y$ . As a result of X ray diffraction, diffraction lines other than TiN were observed if the  $y$  value was smaller than 0.2 or exceeded 0.6. The

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resistivity was checked only for the nitrogen content whose y value was 0.2 to 0.6 (included). For this nitrogen content, a single phase was observed in the X ray diffraction pattern. The resistivity increased as the y value increased. And, the resistivity increased sharply around 0.6 of the y value. Usually, an effect of the impurity phase is observed in the resistivity more than in X ray diffraction. Thus, the threshold values of both x and y to be determined by a resistivity seems to be narrowed.

Next, a platinum layer with a thickness of 30nm was formed by the DC sputtering method on the aluminum titanium layer formed above. The film deposition conditions were as follows: Incident power; 400W, discharge gas; Argon gas, gas pressure; 20 mTorr, and deposition temperature; 500 °C. On the platinum layer was stacked an oxide dielectric layer [Pb(Zr<sub>0.5</sub>Ti<sub>0.5</sub>)O<sub>3</sub>] with a thickness of 100nm, using RF-magnetron sputtering. The film deposition conditions were as follows: temperature of the substrate heater; 300 °C, incident power; 1.5W/cm<sup>2</sup>, deposition rate; 3 nm/min, discharge Ar gas/oxygen gas flow ratio; 90/10, and pressure; 5 mTorr. After the 100nm thick oxide dielectric layer was formed, rapid thermal annealing was applied to the layer at 650 °C for 2 minutes in an oxygen flow, thereby to accelerate the crystallization of the layer.

Finally, the oxide dielectric layer, after it was formed once, was removed completely in a dry etching process, thereby exposing the platinum layer again. An X ray diffraction measurement was made for this sample to check if the aluminum titanium nitride  $[(\text{Ti}_{1-x}\text{Al}_x)_{1-y}\text{N}_y]$  layer was oxidized and changed in quality by the formed oxide dielectric layer. Fig.10 also shows this result. As shown in Fig.10(a), it was confirmed that the oxide layer was oxidized, thereby  $\text{TiO}_2$  was formed when the aluminum content  $x$  was smaller than 0.2. And, as shown in Fig.10(b),  $\text{TiO}_2$  was also observed when the nitrogen content  $y$  was smaller than 0.4.

The above threshold values remained the same even when both aluminum and nitrogen contents  $x$  and  $y$  were fixed at another value respectively.

The above threshold values also remained the same substantially even when platinum was replaced with any of iridium, ruthenium, and rhenium for forming the metallic layer. And, the aluminum titanium nitride layer for preventing oxygen diffusion and oxidation was also effective to other oxide dielectrics, for example, lead zirconate titanate having a different titanium/zirconium ratio, lead barium zirconate titanate, barium strontium titanate, and bismuth ferroelectrics.

<Fifth Embodiment>

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In the fifth embodiment of the present invention, the polarization hysteresis curve of an oxide dielectric capacitor including an aluminum titanium nitride layer for preventing oxygen diffusion and oxidation was measured.

For the sample (a), an oxide dielectric layer was stacked directly on the platinum layer of 30nm in thickness/aluminum titanium nitride layer of 50nm in thickness/conductive silicon substrate described in the fourth embodiment of the present invention. For the sample (b), an oxide dielectric layer was stacked on the above layer through a conductive oxide layer.

A  $\text{RuO}_2$  layer of 50nm in thickness was formed as the conductive oxide layer using the RF-magnetron sputtering method. The target was an Ru metal one. The film deposition conditions were as follows: temperature of the substrate heater; 500 °C, incident power; 1.5W/cm<sup>2</sup>, deposition rate; 3 nm/min, discharge Ar gas/oxygen gas flow ratio; 50/50, and pressure; 7 mTorr.

Lead zirconate titanate [  $\text{Pb}(\text{Zr}_{0.5}\text{Ti}_{0.5})\text{O}_3$  ] layer of 100nm in thickness was formed as the oxide dielectric layer using the sol-gel method. Sol was a solution obtained by making lead acetate, titanium isopropoxide and zirconium isopropoxide react to each other in methoxy ethanol. This solution was coated on the platinum layer [sample (a)] or on the conductive oxide layer [sample (b)], then rapid

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thermal annealing was applied to each sample at 650 °C for two minutes in an oxidizing atmosphere, thereby crystallizing the sample.

A 2mm diameter platinum layer was formed as the upper electrode layer through a metallic mask using the DC sputtering method.

Fig.11 shows a polarization hysteresis curve appeared and measured when a voltage was applied to between the upper electrode layer and the conductive silicon substrate. For both samples (a) and (b), good hysteresis curves were obtained. Even when the platinum layer put therebetween was as thin as 30nm, the aluminum titanium nitride layer functioned effectively to prevent oxygen diffusion and oxidation. It was thus confirmed that the object capacitor operation was satisfactory with a voltage supplied from the substrate.

To select the materials of a conductive oxide layer and an oxide dielectric layer is not essential in the embodiments of the present invention. For example, any of the conductive oxides of  $\text{IrO}_2$ ,  $\text{SrRuO}_3$ , and  $\text{ReO}_3$  can be used to obtain the same effect. In addition, any of lead zirconate titanate  $[\text{Pb}(\text{Zr}_x\text{Ti}_{1-x})\text{O}_3]$  with  $x$  other 0.5, strontium barium titanate  $[(\text{Ba}_x\text{Sr}_{1-x})\text{TiO}_3](x=0 \text{ to } 1)$ , lead barium zirconate titanate, and bismuth layered

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ferroelectrics can be used to form the object capacitor in the same way.

As described in each of the embodiments of the present invention, if an aluminum titanium nitride layer for preventing oxygen diffusion and oxidation, which is one of the characteristics of the present invention, was formed, then the lower electrode layer and the oxide dielectric layer could be formed without oxidizing the nitride layer even when adjacent metallic layers including the platinum one were thinned down to 30nm. Consequently, the interfacial resistance and the contact resistance of each electrode, as well as the capacitor aspect ratio could be reduced, thereby forming an oxide dielectric capacitor suitable for high integration.

## 2. How to Form a Semiconductor Device Provided with a Dielectric Capacitor

Next, description will be made for how an oxide dielectric capacitor of the present invention is used in a semiconductor device. A MOS transistor formed on a silicon substrate will be picked up as an example for the description with reference to the accompanying drawings with respect to the sixth to tenth embodiments of the present invention to be described below. The sixth to eight and ninth to tenth embodiments are based on the guideline 1 and 2 for selecting conductive materials respectively as described above.

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<Sixth Embodiment>

In this sixth embodiment of the present invention, description will be made at first for the pre-process up to the forming of an oxide dielectric capacitor with respect to the manufacturing method of a semiconductor device.

At first, description will be made for how to form a MOS transistor on a silicon substrate, then how to planarize the surface of the substrate once and finally for how to form a polycrystalline silicon plug used to connect the capacitor electrode electrically to the MOS transistor. The series of manufacturing processes will be described sequentially with reference to Figs. 12 to 15.

As shown in Fig. 12, a switching transistor is formed in an existing MOSFET integrating process. 121 is a p-type semiconductor substrate, 122 is an isolating insulator between devices, 123 is a gate oxide film, 124 is a word line used as a gate electrode, and 125 and 126 are n-type impurity diffusion layers in which phosphorus is doped respectively. 127 is passivation layer consisting of  $\text{SiO}_2$ . Next, the surface is covered completely with a 50nm thick  $\text{SiO}_2$  layer 128 by the chemical vapor deposition. After this, the surface is covered once with a 600nm thick  $\text{Si}_3\text{N}_4$  layer 129, then this  $\text{Si}_3\text{N}_4$  layer 129 is etched as deep as the deposited film thickness, thereby filling the insulator between word lines. The structure is thus formed as shown in Fig. 12. The

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$\text{SiO}_2$  layer 128 is an under layer for producing the bit lines in a subsequent process and used to prevent exposed surface of the substrate, as well as damaged isolating insulator 122 between elements.

Fig.13 shows the next process. The  $\text{Si}_3\text{N}_4$  portion where a bit line to be formed later will come in contact with the n-type impurity diffusion layer 125 on the surface of the substrate, as well as the  $\text{Si}_3\text{N}_4$  portion where a capacitor electrode to be formed later will come in contact with the n-type impurity diffusion layer 126 on the surface of the substrate are processed respectively so as to be perforated with holes using the photo-lithography method and the dry etching method. After this, amorphous silicon including n-type impurity is deposited with a thickness of 600nm all over the portion including the holes, then annealed so as to be crystallized. The polycrystalline silicon is then etched as deep as the film thickness, so as to be structured as shown in Fig.13. Consequently, the holes are filled with polycrystalline silicon 131 and 132.

Fig.14 shows the next process for forming a bit line. At first, the entire surface is covered with the  $\text{SiO}_2$  insulator 141 using the chemical vapor deposition. Then, the  $\text{SiO}_2$  insulator positioned above the polycrystalline silicon 131 is perforated with holes using both photo-lithography method and dry etching method so that the bit

line to be formed later are connected to the n-type impurity diffusion layer 125 electrically. After this, metallic silicide to become a bit line later, as well as a polycrystalline silicon layer (142) are formed all over these holes. And, on the layer 142 is deposited an  $\text{SiO}_2$  layer 143 with a thickness of 200nm. The  $\text{SiO}_2$  layer 143, the metallic silicide, and the polycrystalline silicon layer 142 are then patterned using both photo-lithography and dry-etching methods, thereby forming a bit line 142 and an  $\text{SiO}_2$  layer 143. Then, to insulate the side wall of the bit line 142,  $\text{Si}_3\text{N}_4$  is deposited with a thickness of 150nm using the chemical vapor deposition, then etched using the dry-etching method, thereby forming an  $\text{Si}_3\text{N}_4$  side wall spacer 144. Finally, the  $\text{SiO}_2$  insulator 141 positioned above the polycrystalline silicon 132 is treated using both photo-lithography and dry-etching methods, thereby making holes. These holes are used to connect a capacitor electrode to be formed later to the n-type impurity diffusion layer 126 electrically.

Fig. 15 shows the process for planarizing the surface of the substrate and forming a conductive polycrystalline silicon plug before the object capacitor is formed. At first, an insulator 151 is deposited on the substrate with a thickness enough to planarize the surface of the substrate. In this embodiment of the present invention, a

500nm thick boron phosphorus silicate glass (BPSG) is used, but another silicon oxide film may be used instead of the BPSG. The glass is planarized by chemical mechanical polishing. The surface of the substrate can also be covered by  $\text{SiO}_2$  using the chemical vapor deposition, then etched back to planarize the surface. Next, the photo-lithography and the dry etching method are applied to the insulator 151 positioned above the n-type impurity diffusion layer 126, thereby making contact holes. After this, phosphorus-doped amorphous silicon is deposited all over the surface including these holes with a thickness of 200nm using the chemical vapor deposition, then annealed to crystallize the surface. The surface is then etched back using the dry etching method, thereby forming each polycrystalline silicon plug 152 filled with polycrystalline silicon.

This completes the pre-process for forming the oxide dielectric capacitor.

Next, description will be made for respective processes for forming an oxide dielectric capacitor including a double-layered conductive oxide later on the substrate for which a MOS transistor and a polycrystalline silicon plug are already formed. In this embodiment, the lower electrode takes a structure in which a conductive oxide layer with oxygen deficiency is formed directly on the polycrystalline silicon shown in Fig. 2.

At first, as shown in Fig.16, a 10nm thick conductive oxide layer 161 ( $\text{RuO}_2$ ) with oxygen deficiency is formed in an Ar atmosphere using the RF-magnetron sputtering method as described in detail in the first embodiment of the present invention. Then, oxygen is introduced at a gas flow ratio up to  $\text{Ar}/\text{O}_2=9/1$ , as well as the total pressure is increased, thereby stacking a 50nm thick conductive oxide layer 162 so as to form a double-layered conductive oxide layer (161 and 162). After this, the layer (161 and 162) was covered with a 50nm thick W film using the DC sputtering method. Then, a photo resist masking pattern was transferred onto the surface of the layer (161 and 162) using the dry etching method. This transferred pattern was used as a mask to pattern the double-layered conductive oxide layer (161 and 162) using the sputtering etching method. Then, the transferred mask was removed by etching and an oxide dielectric layer 163 was formed. In the embodiments of the present invention, lead zirconate titanate  $[\text{Pb}(\text{Zr}_{0.5}\text{Ti}_{0.5})\text{O}_3]$  was used as oxide dielectrics. The deposition method was as described in detail in the second and third embodiments of the present invention. The film thickness was 100nm. Finally, a platinum cell plate electrode 164 was formed to complete the object memory cell capacitor.

The polarization hysteresis characteristics of the oxide ferroelectric capacitor (sample) were measured by

changing the capacitor area from 0.2 to 25  $\mu\text{m}^2$ . As a result, a satisfactory hysteresis curve was obtained, enabling a voltage to be supplied to the oxide dielectric layer from the polycrystalline silicon plug 152 in any cases.

In the embodiments of the present invention, it is not essential whether to select an oxide dielectric layer. Any of lead zirconate titanate  $[\text{Pb}(\text{Zr}_x\text{Ti}_{1-x})\text{O}_3]$  with  $y$  other than 0.5, strontium barium titanate  $[(\text{Ba}_x\text{Sr}_{1-x})\text{TiO}_3(x=0 \text{ to } 1)]$ , lead barium zirconate titanate, and bismuth layered ferroelectrics can be used to form memory cells in the same way. In addition, the same effect could be obtained for the conductive oxide layer using any of the compounds described in the first embodiment of the present invention.

#### <Seventh Embodiment>

In this seventh embodiment of the present invention, description will be made for a process for forming an oxide dielectric capacitor on a substrate after finishing the processes from forming a MOS transistor up to forming a polycrystalline silicon plug as described in detail in the sixth embodiment of the present invention. The capacitor includes a double-layered conductive oxide layer formed on an anti-diffusion non-oxide conductive layer as shown in Fig. 3.

At first, as shown in Fig. 17, an anti-diffusion oxide conductive layer 171 is formed. In this embodiment, TiN is

used for the anti-diffusion non-oxide conductive layer and such an example will be described in detail. However, note that the same effect was also obtained for the semiconductor device of the present invention when any of the nitrides of Ta, Zr, Nb, V, and W was used. The nitride layer, as described in detail in the second embodiment of the present invention, was formed using the DC sputtering method that used a metallic target. The film thickness was 40nm. After the film deposition, the sample was annealed at 800 °C for two minutes in an ammonia gas atmosphere using the rapid thermal annealing method, thereby accelerating the crystallization of the film.

Next, an  $\text{SrRuO}_3$  layer was formed in a weak oxidizing atmosphere using the RF-magnetron sputtering method. The layer was used as a double-layered conductive oxide layer. The same effect can be obtained even with the film deposition in an Ar gas atmosphere. Then, a conductive oxide layer 161 ( $\text{SrRuO}_3$ ) with a 10nm thick oxygen deficient layer was formed at a gas flow ratio of  $\text{Ar}/\text{O}_2=100/1$ , then the gas flow ratio was lowered to  $\text{Ar}/\text{O}_2=9/1$  thereby stacking a 50nm conductive oxide layer 162 so as to form the double-layered conductive oxide layer (161 and 162). The film deposition conditions including the temperature were the same as those in the second embodiment of the present invention described above.

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Next, the above layers were covered with a 50nm W film and a photo-resist masking pattern was transferred to the W film using the dry etching method. This transferred pattern was used as a mask for patterning the double-layered conductive oxide layer (161 and 162), as well as the anti-diffusion non-oxidizing conductive layer 171 through sputter-etching. The transferred mask was then removed and an oxide dielectric layer 163 was formed. In the embodiments of the present invention, lead zirconate titanate  $[Pb(Zr_{0.5}Ti_{0.5})O_3]$  was used as oxide dielectrics. The film deposition method was the same as those described in the second and third embodiments of the present invention in detail. The film thickness was 100nm. Finally, a platinum electrode 164 was formed to complete the object capacitor of a memory cell.

The sample was then measured with respect to the polarization hysteresis characteristics of this oxide ferroelectric capacitor by changing the capacitor area from 0.2 to 25  $\mu m^2$ . As a result, it was found in any cases that a voltage could be supplied from the polycrystal silicon plug 152 to the oxide dielectric layer so as to obtain a satisfactory hysteresis curve.

In the embodiments of the present invention, it is not essential whether to select an oxide dielectric layer. Any of lead zirconate titanate  $[Pb(Zr_xTi_{1-x})O_3]$  with x other than

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0.5, strontium barium titanate  $[(Ba_xSr_{1-x})TiO_3(x=0 \text{ to } 1)]$ , lead barium zirconate titanate, and bismuth layered ferroelectrics can be used to form memory cells. The same effect could also be obtained using any of the compounds,  $IrO_2$ ,  $RuO_2$ ,  $CaRuO_3$ ,  $SrTiO_3$  to which La is added, and  $ReO_3$  for the conductive oxide layer as described in the first to this embodiments of the present invention.

<Eighth Embodiment>

In this eighth embodiment of the present invention, description will be made for a process for forming an oxide dielectric capacitor on a substrate after finishing the processes from forming of a MOS transistor up to forming of a polycrystalline silicon plug as described in detail in the sixth embodiment of the present invention. The capacitor includes a double-layered conductive oxide layer formed on an anti-diffusion non-oxide conductive layer through a metallic layer as shown in Fig.4.

At first, as shown in Fig.18, an anti-diffusion oxide conductive layer 171 is formed. In this embodiment, TiN is used for the anti-diffusion non-oxide conductive layer and such an example will be described below. However, note that the same effect was also obtained for the semiconductor device of the present invention when any of the nitrides of Ta, Zr, Nb, V, and W was used. The TiN layer was formed as described in detail in the seventh embodiment of the present

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invention. On this layer was further formed a 20nm thick metallic layer 181 using the DC sputtering method. Although platinum was used in this embodiment, it was confirmed that the same effect was also obtained with the use of iridium and ruthenium. The film deposition conditions for the metallic layer were the same as those in the third embodiment of the present invention.

Next, an  $\text{IrO}_2$  layer was formed in a weak oxidizing atmosphere using the RF-magnetron sputtering method. The layer was used as a double-layered conductive oxide layer. Of course, the same effect was obtained even with the film deposition in an Ar gas atmosphere. Then, a 10nm conductive oxide layer 161 ( $\text{IrO}_2$ ) with oxygen deficiency was formed at a gas flow ratio of  $\text{Ar}/\text{O}_2=100/1$ , then the gas flow ratio was lowered to  $\text{Ar}/\text{O}_2=9/1$  so as to stack a 50nm conductive oxide layer 162( $\text{IrO}_2$ ), thereby forming a double-layered conductive oxide layer (161 and 162). The film deposition conditions including the temperature were the same as those in the third embodiment of the present invention described above.

Next, the above layer was covered with a 50nm W film and a photo-resist masking pattern was transferred to the W film using the dry etching method. As this transferred pattern mask was used for patterning the double-layered conductive oxide layers 161 and 162 and metallic layer 181,

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as well as the anti-diffusion non-oxidizing conductive layer 171 through sputter-etching. The transferred mask was then removed and an oxide dielectric layer 163 was formed. In the embodiments of the present invention, lead zirconate titanate [  $\text{Pb}(\text{Zr}_{0.5}\text{Ti}_{0.5})\text{O}_3$  ] was used as oxide dielectrics. The film deposition method was the same as those described in the second and third embodiments of the present invention in detail. The film thickness was 100nm. Finally, a platinum cell plate electrode 164 was formed to complete the object capacitor of a memory cell.

The sample was then measured with respect to the polarization hysteresis characteristics of this oxide ferroelectric capacitor by changing the capacitor area from 0.2 to 25  $\mu\text{m}^2$ . As a result, it was found in any cases that a voltage could be supplied from the polycrystal silicon plug 152 to the oxide dielectric layer so as to obtain a satisfactory hysteresis curve.

In the embodiments of the present invention, it is not essential whether to select an oxide dielectric layer. Any of lead zirconate titanate [  $\text{Pb}(\text{Zr}_x\text{Ti}_{1-x})\text{O}_3$  ] with X other than 0.5, strontium barium titanate [  $(\text{Ba}_x\text{Sr}_{1-x})\text{TiO}_3$  (x=0 to 1) ], lead barium zirconate titanate, and bismuth layered ferroelectrics can be used to form memory cells in the same way. The same effect could also be obtained using any of the compounds,  $\text{RuO}_2$ ,  $\text{SrRuO}_3$ ,  $\text{CaRuO}_3$ ,  $\text{SrTiO}_3$  to which La is

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added, and  $\text{ReO}_3$  as described in the first to third embodiments of the present invention for the conductive oxide layer.

<Ninth Embodiment>

In this ninth embodiment of the present invention, description will be made for a process for forming an oxide dielectric capacitor on a substrate after finishing the processes from forming of a MOS transistor up to forming of a polycrystalline silicon plug as described in detail in the sixth embodiment of the present invention. The capacitor includes an aluminum titanium nitride layer for preventing oxygen diffusion and oxidation. In this embodiment, the lower electrode layer takes a structure in which a metallic layer and an oxide dielectric layer are stacked sequentially on the aluminum titanium nitride shown in Fig. 5.

At first, as shown in Fig. 19, an aluminum titanium nitride  $[(\text{Ti}_{0.7}\text{Al}_{0.3})_{0.5}\text{N}_{0.5}]$  layer 191 was formed using the RF-magnetron sputtering method. The target was a composite one obtained by putting a proper amount of aluminum nitride plate on a titanium nitride plate. The film deposition conditions were as follows: temperature of the substrate heater;  $550^\circ\text{C}$ , incident power; 400W, total gas pressure; 8 mTorr, argon discharge gas/nitrogen gas flow ratio; 90/10, deposition rate; 10 nm/min, and film thickness; 50nm. The

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same effect to be described below was also obtained using another aluminum or nitrogen content described in Fig. 5.

On this layer was further formed a 30nm thick metallic layer 181 using the DC sputtering method. Although platinum was used in this embodiment, it was confirmed that the same effect was also obtained with the use of iridium and ruthenium. The film deposition conditions for the metallic layer were the same as those in the fourth embodiment of the present invention.

Next, the layer formed above was covered with a 50nm W film and a photo-resist masking pattern was transferred to the W film using the dry etching method. Using this transferred pattern as a mask, the aluminum titanium nitride layer 191 and the metallic layer 182 were patterned through sputter-etching. The transferred mask was then removed and an oxide dielectric layer 163 was formed. In the embodiments of the present invention, lead zirconate titanate  $[Pb(Zr_{0.5}Ti_{0.5})O_3]$  was used as oxide dielectrics. The film deposition method was the sol-gel method as described in the fifth embodiment of the present invention in detail. The film thickness was 100nm. Finally, a platinum electrode 164 was formed and patterned to complete the object capacitor of a memory cell.

The sample was then measured with respect to the polarization hysteresis characteristics of this oxide

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ferroelectric capacitor by changing the capacitor area from 0.2 to 25  $\mu\text{m}^2$ . As a result, it was found in any cases that a voltage could be supplied from the polycrystal silicon plug 152 so as to obtain a satisfactory hysteresis curve.

In the embodiments of the present invention, it is not essential whether to select an oxide dielectric layer. Any of lead zirconate titanate  $[\text{Pb}(\text{Zr}_x\text{Ti}_{1-x})\text{O}_3]$  with x other than 0.5, strontium barium titanate  $[(\text{Ba}_x\text{Sr}_{1-x})\text{TiO}_3 (x=0 \text{ to } 1)]$ , lead barium zirconate titanate, and bismuth layered ferroelectrics can be used to form memory cells in the same way.

<Tenth Embodiment>

In this tenth embodiment of the present invention, description will be made for a process for forming an oxide dielectric capacitor on a substrate after finishing the processes from forming of a MOS transistor up to forming of a polycrystalline silicon plug as described in detail in the sixth embodiment of the present invention. The capacitor includes an aluminum titanium nitride layer for preventing oxygen diffusion and oxidation. In this embodiment, the lower electrode layer takes a structure in which a metallic layer, a conductive oxide layer, and an oxide dielectric layer were stacked sequentially on the aluminum titanium nitride shown in Fig. 5.

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At first, as shown in Fig.20, an aluminum titanium nitride  $[(Ti_{0.5}Al_{0.5})_{0.5}N_{0.5}]$  layer 191 and a metallic layer 181 were formed using the same method as that in the ninth embodiment. The same effect to be described below was also obtained using another aluminum or nitrogen content, as well as using iridium, ruthenium, and rhenium.

A 50nm thick  $IrO_2$  layer formed using the RF-magnetron sputtering method was used as the conductive oxide layer 201. The target was an Ir metal one. The film deposition conditions were as follows: temperature of the substrate heater; 500 °C, incident power; 1.5W/cm<sup>2</sup>, deposition rate; 3 nm/min, discharge Ar gas/oxygen gas flow ratio; 50/50, and pressure; 7 mTorr.

Next, the layer formed above was covered with a 50nm W film and a photo-resist masking pattern was transferred to the W film using the dry etching method. Using this transferred pattern as a mask, the aluminum titanium nitride layer 191, the metallic layer 181, as well as a conductive oxide layer 201 were patterned through sputter-etching.

The transferred mask was then removed and an oxide dielectric layer 163 was formed. In the embodiments of the present invention, bismuth layered ferroelectrics,  $Bi_4Ti_3O_{12}$ , was used as oxide dielectrics. In an oxidizing atmosphere at 50  $\mu$ Torr in pressure, the titanium and bismuth were evaporated using an electron gun and an effusion cell

respectively, thereby forming a 100nm thick amorphous oxide layer in the room temperature. After this, a rapid thermal annealing treatment was applied to the sample at 700 °C for 2min in an oxygen atmosphere so as to crystallize the surface. Finally, a platinum cell plate electrode 164 was formed and patterned to complete the object capacitor of a memory cell.

The sample was then measured with respect to the polarization hysteresis characteristics of this oxide ferroelectric capacitor by changing the capacitor area from 0.2 to 25  $\mu\text{m}^2$ . As a result, it was found in any cases that a voltage could be supplied from the polycrystal silicon plug 152 to the oxide dielectric layer so as to obtain a satisfactory hysteresis curve.

Whether to select a conductive oxide layer or an oxide dielectric layer is not essential in the embodiments of the present invention. In addition, any of lead zirconate titanate  $[\text{Pb}(\text{Zr}_x\text{Ti}_{1-x})\text{O}_3](x=0 \text{ to } 1)$ , strontium barium titanate  $[(\text{Ba}_x\text{Sr}_{1-x})\text{TiO}_3](x=0 \text{ to } 1)$ , lead barium zirconate titanate, bismuth layered ferroelectrics, and  $\text{SrBi}_2\text{Ta}_2\text{O}_9$  can be used to form the object capacitor in the same way. Any of the conductive oxides of  $\text{RuO}_2$ ,  $\text{SrRuO}_3$ ,  $\text{ReO}_3$  can also be used to obtain the same effect.

As described in each of the embodiments of the present invention, a MOS transistor formed on a silicon substrate

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is applied to a semiconductor device provided in an oxide dielectric capacitor of the present invention. As for the guideline 1 for selecting conductive materials, a conductive oxide layer with oxygen deficiency was formed in a non-oxidizing atmosphere, thereby forming a double-layered conductive oxide layer. Consequently, the object memory cell was formed without oxidizing the polycrystalline silicon (the sixth embodiment of the present invention) adjacent to the double-layered conductive oxide layer, the anti-diffusion non-oxide conductive layer consisting of a nitride, etc. (the seventh embodiment of the present invention), and the anti-diffusion non-oxide conductive layer (the eighth embodiment of the present invention) through a metallic layer. In accordance with the guideline 2 for selecting conductive materials, an aluminum titanium nitride layer for preventing oxygen diffusion and oxidation was formed, thereby stacking an oxide dielectric layer (the ninth embodiment of the present invention) and a conductive oxide layer (the tenth embodiment of the present invention) without oxidizing the nitride layer even when the metallic layer consisting of platinum, etc. and adjacent to the aluminum titanium nitride layer for preventing oxygen diffusion and oxidation was thinned down to 30nm. The object memory cell could be formed such way. According to the

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structures and film deposition methods described above, it became possible to reduce both interfacial resistance and contact resistance of the object electrode, as well as to reduce the capacitor aspect ratio. It was thus possible for the present invention to obtain a semiconductor device provided with fine-structured memory cells suitable for high integration.

In the above embodiments of the present invention, the semiconductor of the present invention was mainly applied to a MOSFET. The semiconductor can also be applied to other devices that use oxide dielectrics (including oxide ferroelectrics) as a capacitor, for example, a GaAs MMIC that uses oxide dielectrics as a so-called path condensor and a chip condensor.

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CLAIMS

1. A semiconductor device, comprising:

a substrate;

a lower electrode layer formed on said substrate;

an oxide dielectric layer formed on said lower

electrode layer; and

an upper electrode layer formed on said oxide dielectric layer, wherein

said lower and upper electrode layers, as well as said oxide dielectric layer are combined to compose an oxide dielectric capacitor, said lower electrode layer includes a conductive oxide layer, said conductive oxide layer consists of two adjacent layers formed in the same crystal structure and with the same elements, but differently in the composition ratio from each other, and one of said two adjacent layers, which is positioned at said substrate side, includes oxygen deficiency.

2. A semiconductor device in accordance with claim 1, wherein

a MOS transistor is disposed on said substrate, and said lower electrode layer is connected electrically to the source area or drain area of said MOS transistor.

3. A semiconductor device in accordance with claim 1, wherein

said lower electrode layer consists of a conductive silicon layer, a conductive oxide layer with oxygen deficiency, and a conductive oxide layer that are stacked sequentially from said substrate side.

4. A semiconductor device in accordance with claim 1, wherein

said lower electrode layer consists of a conductive silicon layer, a non-oxide conductive layer for anti-diffusion, a conductive oxide layer with oxygen deficiency, and a conductive oxide layer that are stacked sequentially from said substrate side.

5. A semiconductor device in accordance with claim 4, wherein

a metallic layer is further formed between said anti-diffusion non-oxide conductive layer and said conductive oxide layer with oxygen deficiency, said metallic layer is composed of at least one type metal selected from a group of platinum, ruthenium, and iridium.

6. A semiconductor device in accordance with claim 4, wherein

said anti-diffusion non-oxide conductive layer consists of a nitride including at least one type metal selected from a group of Ti, Ta, Zr, Nb, V, and W.

7. A semiconductor device in accordance with claim 1, wherein

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an oxide composing said double-layered conductive oxide layer is at least one type compound selected from  $\text{RuO}_2$  and  $\text{IrO}_2$  having the rutile structure.

8. A semiconductor device in accordance with claim 7, wherein

said conductive oxide layer with said oxygen deficiency, which has said rutile structure, is characterized by that the oxygen deficiency  $x$  in its chemical formula  $\text{MO}_{2-x}$  ( $M=\text{Ru}$  or  $\text{Ir}$  element) with said oxygen deficiency is larger than 0 and smaller than a value that can maintain said rutile structure stable.

9. A semiconductor device in accordance with claim 1, wherein

an oxide composing said double-layered conductive oxide layer consists of at least one type compound selected from a group of  $\text{CaRuO}_3$ ,  $\text{SrRuO}_3$ , and  $\text{SrTiO}_3$  to which La is added by over 0.5 weight% to 4.0 weight% (included), and all of them having the perovskite structure.

10. A semiconductor device in accordance with claim 1, wherein

an oxide composing said double-layered conductive oxide layer has a mixed phase of at least one type compound selected from a group of  $\text{CaRuO}_3$ ,  $\text{SrRuO}_3$ , and  $\text{SrTiO}_3$  to which La is added by over 0.5 weight% to 4.0 weight% (included), and all of them having the perovskite structure, with an

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alkaline-earth metal oxide composing said compound, that is, CaO or SrO.

11. A semiconductor device in accordance with claim 9, wherein

said conductive oxide layer with said oxygen deficiency and consisting of an oxide of said perovskite structure is characterized by that the oxygen deficiency  $x$  in its chemical formula  $AMO_{3-x}$  (A and M indicate any of said Ca, Sr, Ti, and La elements) is larger than 0 and smaller than a value that can maintain the perovskite structure stable.

12. A semiconductor device in accordance with claim 1, wherein

said double-layered conductive oxide layer consists of  $ReO_3$ .

13. A semiconductor device in accordance with claim 12, wherein

said conductive oxide layer with said oxygen deficiency and consisting of said  $ReO_3$  is characterized by that the oxygen deficiency  $x$  in its chemical formula  $ReO_{3-x}$  with said oxygen deficiency is larger than 0 and smaller than a value that can maintain the  $ReO_3$  structure stable.

14. A semiconductor device in accordance with claim 1, wherein

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said conductive oxide layer with said oxygen deficiency is 10nm or above in thickness.

15. A semiconductor device in accordance with claim 1, wherein

said oxide dielectric layer is formed with one compound selected from lead zirconate titanate, lead barium zirconate titanate, and strontium barium titanate.

16. A semiconductor device in accordance with claim 1, wherein

said oxide dielectric layer consists of bismuth-system layered ferroelectrics.

17. A method for manufacturing a semiconductor device, including a process for forming a conductive oxide layer with oxygen deficiency by sputtering or evaporating elements composing said conductive oxide in a non-oxidizing atmosphere, then forming a conductive oxide layer on said conductive oxide layer with said oxygen deficiency, thereby forming a lower electrode layer on a substrate; a process for forming an oxide dielectric layer on said lower electrode layer; and a process for forming an upper electrode layer on said oxide dielectric layer, wherein

said lower electrode layer consists mainly of two conductive oxide layers formed in the same crystal structure and consisting of the same element, but different from each other in oxygen composition ratio, and

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said lower and upper electrode layers, as well as said oxide dielectric layer are combined thereby composing an oxide dielectric capacitor.

18. A method for manufacturing a semiconductor device in accordance with claim 17, wherein

at least part of a MOS transistor is formed on said substrate before said lower electrode layer is formed so as to be connected electrically to the source area or drain area of said MOS transistor.

19. A method for manufacturing a semiconductor device in accordance with claim 17, wherein

said conductive oxide layer with said oxygen deficiency formed in said double-layered conductive oxide layer is formed with the sputtering method and said non-oxidizing atmospheric gas is an argon gas (Ar) of 3N (99.9%) or over in purity.

20. A method for manufacturing a semiconductor device in accordance with claim 17, wherein

said conductive oxide layer with said oxygen deficiency, which is formed in said double-layered conductive oxide layer, is then formed with the sputtering method or the vacuum deposition method, and said non-oxidizing atmospheric gas is a vacuum state of 1  $\mu$ Torr or below into which no oxidizing gas consisting of any of oxygen

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(O<sub>2</sub>), nitric monoxide (N<sub>2</sub>O), nitric dioxide (NO<sub>2</sub>), and ozone (O<sub>3</sub>) is introduced intentionally.

21. A method for manufacturing a semiconductor device in accordance with claim 17, wherein

said conductive oxide layer with said oxygen deficiency, which is formed in said double-layered conductive oxide layer, is then formed with the sputtering method or the vacuum deposition method, and said non-oxidizing atmospheric gas consists of at least one type selected from oxygen (O<sub>2</sub>), nitric monoxide (N<sub>2</sub>O), nitric dioxide (NO<sub>2</sub>), and ozone (O<sub>3</sub>), and the pressure or partial pressure of said gas is 10  $\mu$ Torr or below.

22. A semiconductor device, comprising;

a substrate;

a lower electrode layer formed on said substrate;

an oxide dielectric layer formed on said lower electrode layer; and

an upper electrode layer provided on said oxide dielectric layer, wherein

said lower and upper electrode layers, as well as said oxide dielectric layer are combined to compose an oxide dielectric capacitor, and said lower electrode layer includes an aluminum titanium nitride layer.

23. A semiconductor device in accordance with claim 22, wherein

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a MOS transistor is disposed on said substrate, and said lower electrode layer is connected electrically to the source area or drain area of said MOS transistor.

24. A semiconductor device in accordance with claim 22, wherein

said lower electrode layer consists of a conductive silicon layer, an aluminum titanium nitride layer, and a metallic layer that are stacked sequentially from said substrate side.

25. A semiconductor device in accordance with claim 24, wherein

a conductive oxide layer is further formed on said metallic layer in said lower electrode layer.

26. A semiconductor device in accordance with claim 24, wherein

said metallic layer consists of at least one type metal element selected from a group of platinum, iridium, ruthenium, and rhenium.

27. A semiconductor device in accordance with claim 25, wherein

said conductive oxide layer consists of one type compound selected from a group of  $\text{IrO}_2$ ,  $\text{RuO}_2$ ,  $\text{SrRuO}_3$ , and  $\text{ReO}_3$ .

28. A semiconductor device in accordance with claim 22, wherein

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the composition of said aluminum titanium nitride layer is represented by a chemical formula of  $(\text{Ti}_{1-x}\text{Al}_x)_1\text{-yN}_y$ , and x is over 0.2 to 0.5 (included) and y is over 0.4 to 0.6 (included).

29. A semiconductor device in accordance with claim 22, wherein

said oxide dielectric layer is formed with one compound selected from lead zirconate titanate, lead barium zirconate titanate, and strontium barium titanate.

30. A semiconductor device in accordance with claim 22, wherein

said oxide dielectric layer consists of bismuth-system layered ferroelectrics.

31. A method for manufacturing a semiconductor device, including;

a step for forming a lower electrode layer including an aluminum titanium nitride layer on a substrate by sputtering in a nitridizing atmosphere; a step for forming an oxide dielectric layer on said lower electrode layer; and a step for forming an upper electrode layer on said oxide dielectric layer, wherein

both lower and upper electrode layers, as well as said oxide dielectric layer are combined thereby composing an oxide dielectric capacitor.

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32. A method for forming a semiconductor device in accordance with claim 31, wherein

at least part of an MOS transistor is formed on the surface of said substrate before said lower electrode layer is formed, and said lower electrode layer is formed so as to be connected electrically to the source or drain area of said MOS transistor.

33. A method for forming a semiconductor device in accordance with claim 31, wherein

said nitridizing atmosphere used for forming said aluminum titanium nitride layer preventing oxygen diffusion and oxidation includes a nitrogen gas of 10 to 90 mol% in an inactive gas.

34. A method for forming a semiconductor device in accordance with claim 31, wherein

a temperature for forming said aluminum titanium nitride layer preventing oxygen diffusion and oxidation is 550 °C or below.

35. A semiconductor device, including;

first area consisting of a semiconductor material;  
second area connected to said first area and consisting of said first conductive material; third area connected to said second area and consisting of said second conductive material; fourth area connected to said third area and consisting of an oxide dielectric material; and fifth area

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connected to said fourth area and consisting of a conductive material, wherein the material composition at the interface of said first area adjacent to said second area is approximately equal to the average material composition of said first area, and the material compositions at the interface of said second area adjacent to said first area, as well as to said third area is approximately equal to the average material composition of said second area.

36. A semiconductor device, including;

first area consisting of a conductive semiconductor material; second area connected to said first area and consisting of said first conductive material; third area connected to said second area and consisting of said second conductive material; fourth area connected to said third area and consisting of an oxide dielectric material; and fifth area connected to said fourth area and consisting of a conductive material, wherein

the average resistivity of said first area is approximately equal to the resistivity of said semiconductor material and the average resistivity of said second area is approximately equal to the resistivity of said first conductive material.

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### Abstract

The object of the present invention is to provide a method for manufacturing a semiconductor device that uses oxide dielectrics for the capacitor and to suppress the oxidation at the interface of lower electrode of the capacitor. The oxide dielectric capacitor is composed of a lower electrode layer 11, oxide dielectrics 16 positioned on the lower electrode layer 11, and an upper electrode layer 17 positioned on the oxide dielectric layer 16. The lower electrode layer 11 includes a double-layered conductive oxide layer 12. These adjacent two layers 14 and 15 are composed in the same crystal structure and with the same element. The layer 14 positioned at the substrate 10 side includes oxygen deficiency. And, since the conductive oxide layer 14 including oxygen deficiency functions to prevent oxygen diffusion, the component 13 of the lower electrode layer, adjacent to the layer 14, as well as its interface can be prevented from oxidation, thereby assuring a proper electrical connection between them.

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FIG. 1

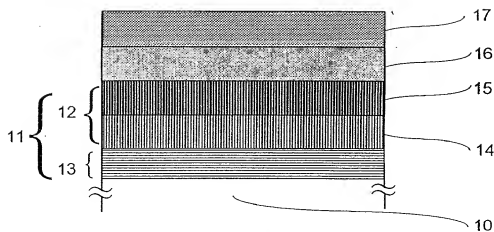


FIG. 2

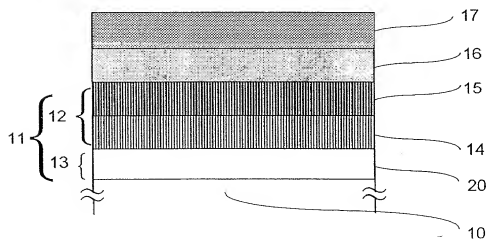


FIG. 3

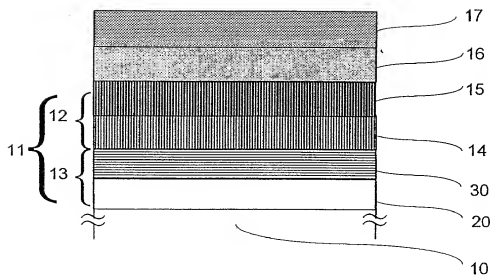


FIG. 4

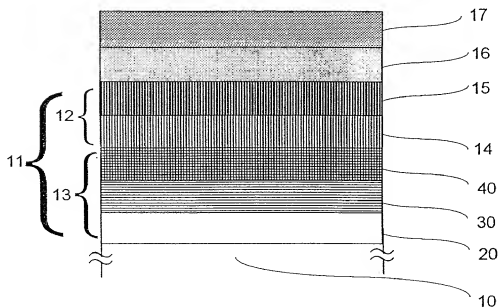


FIG. 5

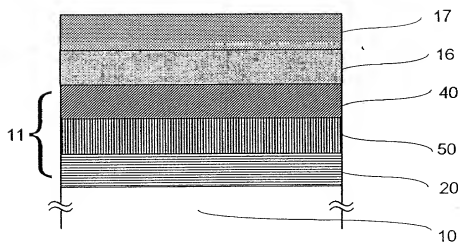


FIG. 6

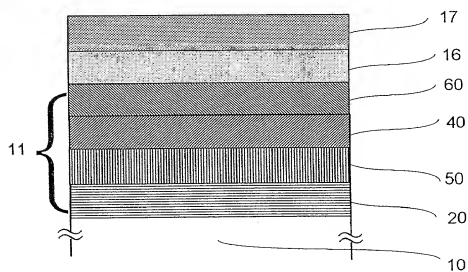
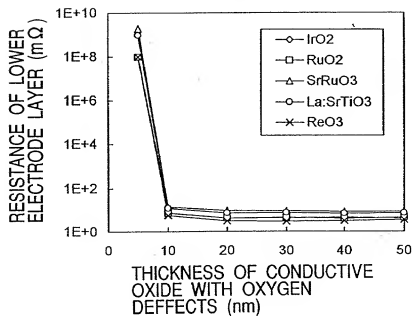


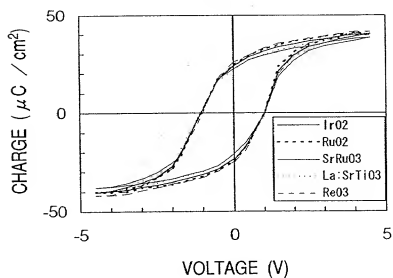


FIG. 7

(a)



(b)



5 / 13

FIG. 8

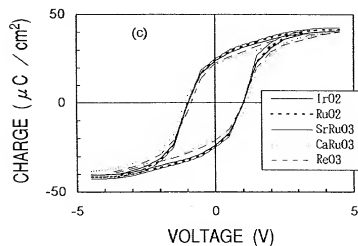
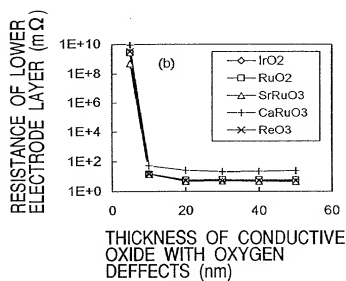
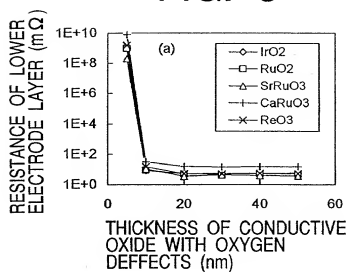


FIG. 9

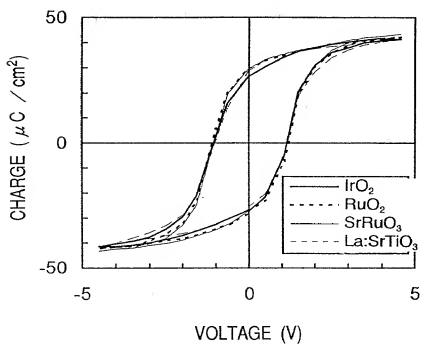
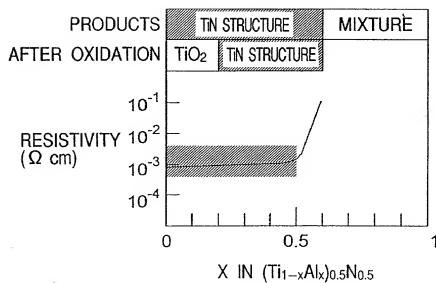


FIG. 10

(a)



(b)

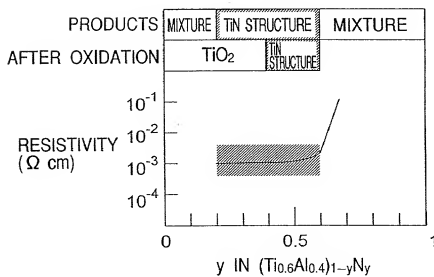
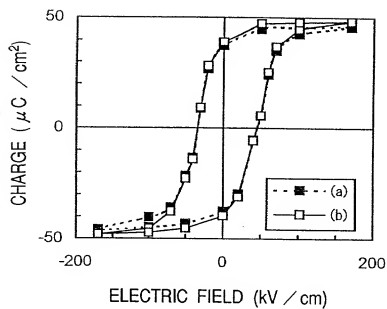


FIG. 11



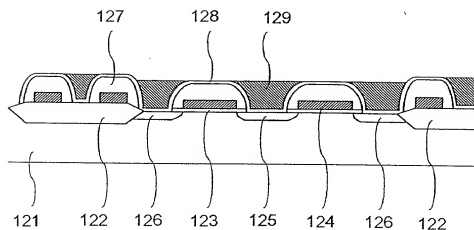
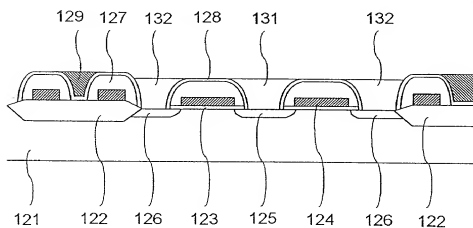
*FIG. 12**FIG. 13*

FIG. 14

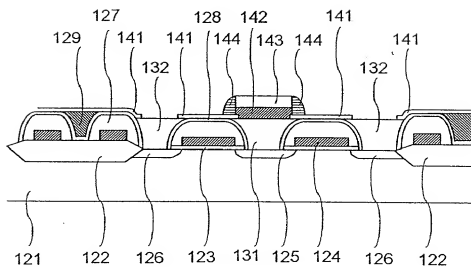


FIG. 15

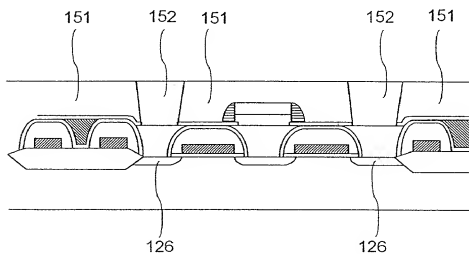


FIG. 16

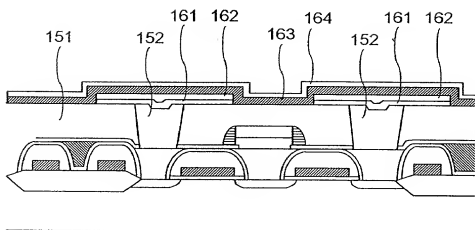


FIG. 17

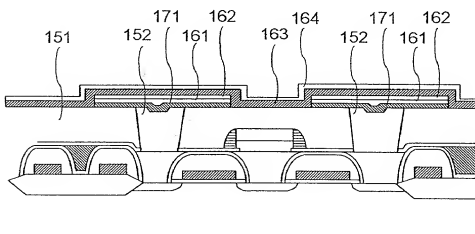




FIG. 18

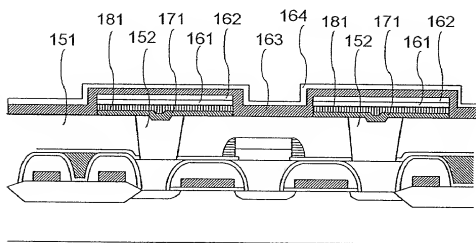


FIG. 19

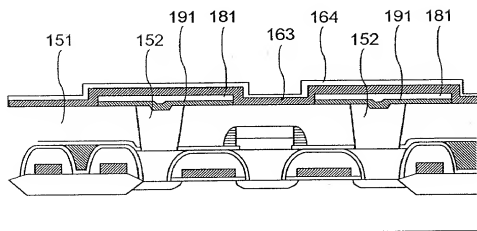
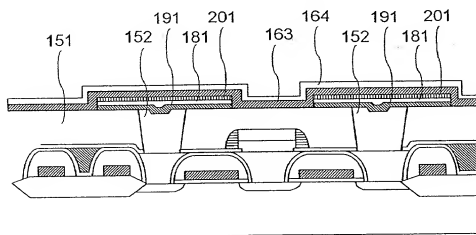


FIG. 20



DECLARATION AND POWER OF ATTORNEY FILED WITH U.S. DESIGNATED OFFICE UNDER 35 U.S.C. 371(c)(4)

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name, I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

SEMICONDUCTOR DEVICE AND ITS MANUFACTURING METHOD

the specification of which was filed as PCT International Application No. PCT/JP96/02226

filed August 7, 1996 and was amended on \_\_\_\_\_ (if applicable)

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, §1.56(a).

I hereby claim foreign priority benefits under Title 35, United States Code, § 119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s)

Priority Claimed

(Number) _____	(Country) _____	(Day/Month/Year Filed) _____	<input type="checkbox"/> Yes	<input type="checkbox"/> No
(Number) _____	(Country) _____	(Day/Month/Year Filed) _____	<input type="checkbox"/> Yes	<input type="checkbox"/> No
(Number) _____	(Country) _____	(Day/Month/Year Filed) _____	<input type="checkbox"/> Yes	<input type="checkbox"/> No
(Number) _____	(Country) _____	(Day/Month/Year Filed) _____	<input type="checkbox"/> Yes	<input type="checkbox"/> No
(Number) _____	(Country) _____	(Day/Month/Year Filed) _____	<input type="checkbox"/> Yes	<input type="checkbox"/> No
(Number) _____	(Country) _____	(Day/Month/Year Filed) _____	<input type="checkbox"/> Yes	<input type="checkbox"/> No

I hereby claim the benefit under Title 35, United States Code, § 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, § 1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

(Application Serial No.) _____	(Filing Date) _____	(Status: patented, pending, abandoned) _____
(Application Serial No.) _____	(Filing Date) _____	(Status: patented, pending, abandoned) _____
(Application Serial No.) _____	(Filing Date) _____	(Status: patented, pending, abandoned) _____
(Application Serial No.) _____	(Filing Date) _____	(Status: patented, pending, abandoned) _____

I hereby appoint as principal attorneys; Donald R. Antonelli, Reg. No. 20,296; David T. Terry, Reg. No. 20,178; Melvin Kraus, Reg. No. 22,466; Stanley A. Wal, Reg. No. 26,432; William I. Solomon, Reg. No. 28,565; Gregory E. Montone, Reg. No. 28,141; Ronald J. Shore, Reg. No. 28,577; Donald E. Stout, Reg. No. 26,422; Alan E. Schiavelli, Reg. No. 32,087; James N. Dresser, Reg. No. 22,973 and Carl I. Brundidge, Reg. No. 29,621 to prosecute and transact all business connected with this application and any related United States application and international applications. Please direct all communications to the following address:

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further, that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United State Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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